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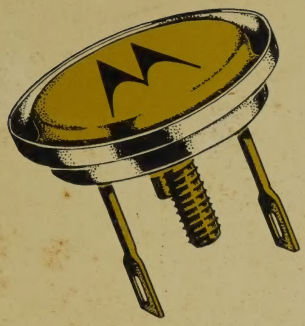


MOTOROLA POWER TRANSISTOR HANDBOOK

- theory
- design characteristics
- applications

This handbook has been compiled by
the Applications Engineering Department
of
Motorola's Semiconductor Products Division.
Edited by
Ralph Greenburg, Group Leader
Industrial Applications.
This department is always available
to help with application problems.

first edition

MOTOROLA
POWER TRANSISTOR HANDBOOK

theory, design characteristics and applications

MOTOROLA
Semiconductor Products Division, Inc.
5005 E. McDowell • Phoenix, Arizona

Circuit diagrams are included as a means of illustrating typical power transistor applications, and the complete information necessary for constructional purposes is not necessarily given. The information in this handbook has been carefully checked, and is believed to be entirely reliable, but no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola, Inc. or others.

CONTENTS

INTRODUCTION

This handbook is intended as a single source of much-needed information covering the proper design of power transistor circuits, specific circuit applications, and areas of promise for future transistor circuit development. The information presented here will be helpful to the design engineer, development engineer, hobbyist, and experimenter.

The power transistor is an extremely efficient and versatile device. Capable of handling large amounts of power, it is nevertheless very compact physically. Circuits have been designed to solve any practical combination of voltage, current, and power requirements. Usable transistor circuits have been designed for series operation at 300 volts and higher, and for parallel operation at current levels exceeding 1000 amperes. One of the first applications of the power transistor was as a replacement for the power output stage in automobile radios. Since the power transistor could work directly from the 12-volt vehicular battery, the vibrator power supply was eliminated. Other early applications for the power transistor were as a replacement for dynamotors or vibrators in D-C to D-C converters.

The power transistor was, in fact, one of the first semiconductor devices to achieve widespread application and production. The diamond-shaped germanium power transistor developed by Motorola in 1954 demonstrated excellent power-handling characteristics as well as a new standard of high reliability. Today, power transistors are found in many types of power supplies, TV sweep circuits, electronic automobile ignition systems, audio amplifiers, and industrial control applications. There are more than 10 million Motorola power transistors in field use, and it is conservatively estimated that these units have registered more than 10 billion hours of operation under extreme environmental operating conditions. Failures have been negligible.

Refinements are continually being made in transistor design and application. For example, Motorola now specifies all of its industrial germanium power transistors for continuous operation at junction temperatures of 100°C. This is a conservative rating, to assure the ultimate in transistor life and reliability. High-temperature storage life tests have been conducted on Motorola units at 125°C without detrimental effects.

It is important that the circuit design engineer thoroughly understand the operating characteristics and ratings of power transistors. It is the purpose of this handbook to provide the background necessary to utilize the characteristics and ratings in designing circuits which will provide completely reliable operation and permit the benefits of transistorized circuits to be more widely utilized.


MOTOROLA, INC. SEMICONDUCTOR PRODUCTS DIVISION

CHAPTER I

Semiconductor Electronics

The transistor has unique amplification characteristics resulting from the electrical properties of a class of elements and compounds known as semiconductors. Semiconductors are so called because they display conductive characteristics intermediate between metals (which are good electrical conductors) and insulators (which are very poor conductors).

At the present time the chemical elements most often used as the basic material in semiconductor devices are germanium and silicon. Both are in Group IV of the periodic table and have four valence electrons in the outer shell. In the crystalline space lattice these electrons join with the valence electrons of neighboring atoms to form a completely saturated system of covalent bonds. This structure is represented schematically in Figure 1-1A. The structure is identical for both germanium and silicon.

Since all the electrons are locked in place in this structure, there are no free electrons to impart conductivity. These materials when very pure are poor electrical conductors, although thermal effects may give a few electrons enough energy to break their bonds and by drifting to conduct electricity in an applied field. The spaces vacated by such electrons—called "holes" in semiconductor terminology—leave a net positive charge on the associated atom. These atoms are not free to move, hence the charge cannot drift with an applied field. However, the atoms may capture a free electron drifting by in a process known as recombination. The captured electron may have originated from another nearby bond, in which case that hole may be said to have moved, thus imparting conductivity.

The conductivity is greatly enhanced by adding controlled amounts of certain impurities. For example, the addition of small amounts of antimony to the pure germanium imparts relatively high conductivity. In this case extra or free electrons are introduced into the semiconductor since the antimony, called a donor impurity, has five valence electrons, only four of which can be shared in the covalent bonds (see Figure 1-1B). This extra electron is free to drift, ionizing the impurity atom. Materials with these excess electrons are called N-type materials. Phosphorus, also a pentavalent element, is generally used as the N-type impurity agent for silicon.

When a trivalent element such as indium is added to germanium (or boron to silicon), the three valence electrons are taken up in the covalent bonds leaving one of the electron bonds in the parent atom unsatisfied. In this manner a positively charged hole exists which can capture electrons drifting by. This is known as P-type material (Figure 1-1C). Both N- and P-type materials are used in transistors and other semiconductor devices.

When P- and N-type materials are brought together, a PN junction is created. In actual practice the PN junction is formed by growing a crystal of either P- or N-type material and in one area alloying or diffusing-in the type of impurity required to create the opposite type of material. When indium is alloyed into the N-type germanium, a small amount of the indium penetrates the germanium and overrides the effect of the antimony, causing areas of the semiconductor slab to become doped P-type.

Although both P- and N-type materials are neutral in charge, the excess electrons in the N-type material are able to cross the interface and combine with the holes in the P-type material. When this occurs, the impurity atoms become ionized. The N-type, upon losing an electron, becomes positively charged and the P-type impurity atom, upon receiving an electron, becomes negatively charged. These ions then form a potential barrier which is negative on the P side and positive on the N side. This potential barrier inhibits further flow of charges across the interface and a state of equilibrium is reached. (See Figure 1-2.)

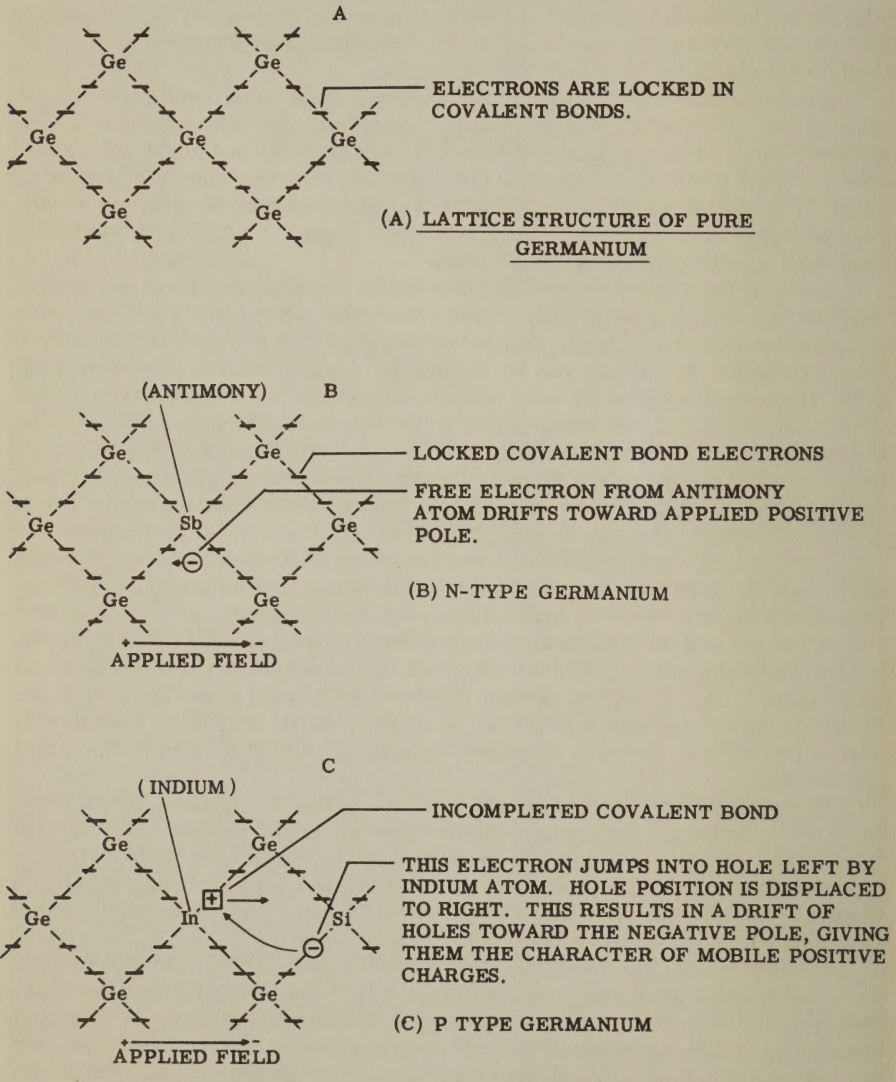


Figure 1-1 — Lattice Structure of Semiconductor Materials

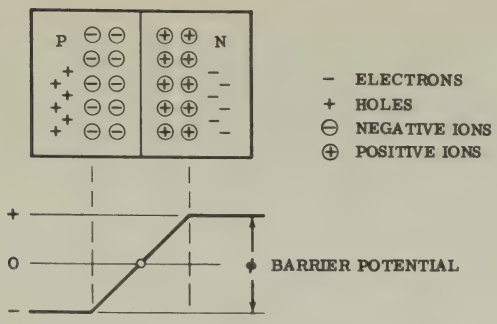


Figure 1-2 — Charge Distribution of PN Junction

It should be noted that the entire crystal is still electrically neutral but a sharp potential difference exists across the interface. At a given temperature only a certain number of electrons will have enough energy to diffuse across this barrier.

To increase the number of electrons that cross the interface, it is necessary to decrease this potential barrier. This can be done by applying a forward bias, using a battery with the positive terminal connected to the P side and the negative terminal connected to the N side. Then some of the ions on both sides lose their charge thereby lowering the barrier potential, as shown in Figure 1-3.

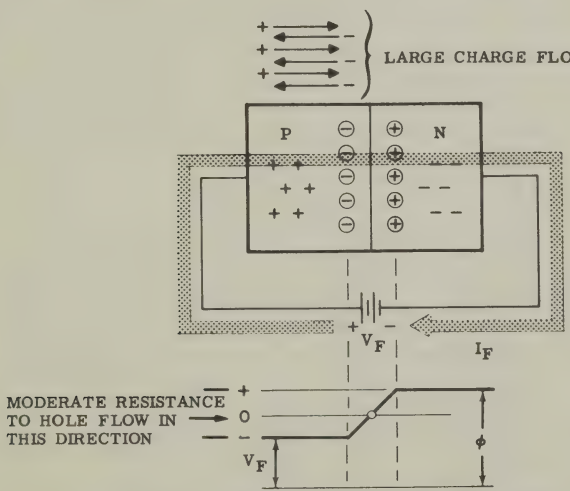


Figure 1-3 — Forward Bias of PN Junction

In Figure 1-4 we have an NP junction with a reverse bias applied: that is the negative terminal of the battery is connected to the P-type material and the positive terminal is connected to the N-type material. The result is an increase in the number of ionized atoms on each side of the interface. Consequently the barrier potential has been increased and the diffusion of charges across the interface is greatly reduced.

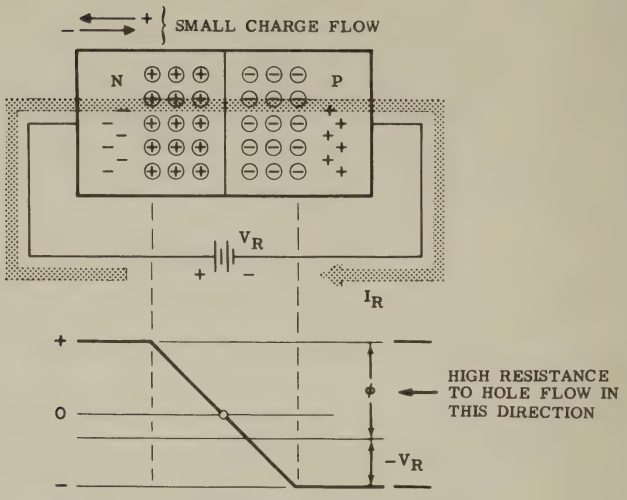


Figure 1-4 — Reverse Bias of NP Junction

When PN and NP junctions are combined, with the N-type region common to both as shown in Figure 1-5, a PNP transistor is created. With a forward bias applied to the PN junction, the number of carriers from the P region (or emitter) which diffuse into the N region (or base) can be modulated by varying the forward bias. If the thickness of the N region or base is small enough, the diffusion of positive carriers will continue through the NP interface. With a reverse bias applied across the NP interface, there is little resistance to the flow of positive carriers. Some of the positive carriers combine with electrons that have entered from the base lead, creating a slight base current flow, I_B. However,

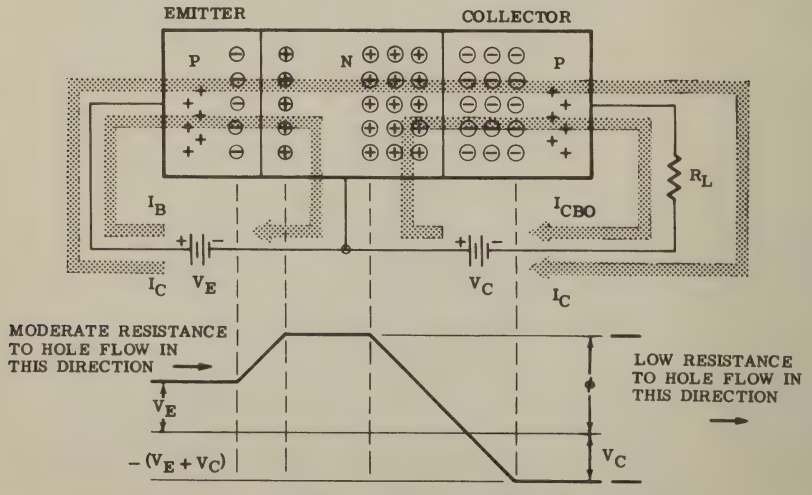


Figure 1-5 — Potential Profile of PNP Transistor

the great majority of positive carriers cross through the collector region into the external circuit. Note that the purpose of the collector bias voltage is not to create current flow but to allow usable power to be delivered to the load resistance. The transistor can be shown to have power gain since a small input power can control a large load power. Consider input power as $I_E^2R_{in}$, where R_{in} is the input resistance of the emitter-base junction. Load power is $I_C^2R_L$ and power gain is

$$G = \frac{P_o}{P_{in}} = \frac{I_C^2R_L}{I_E^2R_{in}}.$$

The emitter-base junction input resistance may be as low as a fraction of an ohm while the typical load resistance may be a thousand times as great. This explains why a transistor can provide a large power gain.

The ratio of I_C/I_E is called the common-base current gain, h_{fb}, which is normally 0.95 - 0.99. To attain higher power gains it is only necessary to increase R_L, as long as there is a specific minimum voltage maintained across the collector and base under D-C and A-C conditions. In the case of an A-C input, the collector voltage swings from a very low to a very high value, approaching the battery voltage. The gain is also a function of the emitter material, base width, and geometry of the device, especially the ratio of collector diameter to emitter diameter. There is a limit to the maximum voltage which can be placed across a junction; additional voltage will cause the charges to avalanche and become dependent upon voltage. At this point, which is known as the breakdown voltage, there is no longer any control of the transistor. This condition is not destructive, however, as long as the current is limited below the safe power point.

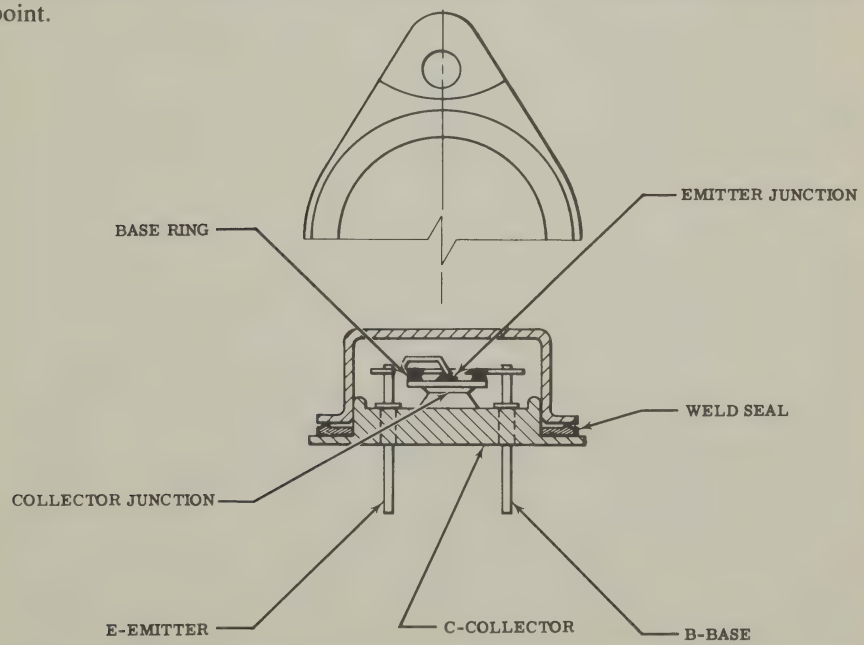


Figure 1-6 — Power Transistor Construction

The P-type emitter is heavily doped and contains a large excess of holes or positive carriers. The N-type base contains a moderate excess of electrons and the collector a small excess of holes.

The interfaces between the regions of different types are considered to be very abrupt and thin, and base width, W, very small compared to the junction diameters.

Since there are many more holes at the interface of the P-type than there are electrons in the N-type, there is a high probability that many holes will penetrate the barrier and diffuse into the base. These will diffuse into the collector because of the very narrow base spacing.

The most common form of transistor is the PNP alloy-junction germanium type. These are fabricated by alloying a suitable impurity into both sides of the die. Other junction-forming techniques include barrier layer, diffused, grown junction, and mesa methods. These procedures are also used to produce NPN transistors.

In manufacturing the transistor, contacts to the die and junctions are made with wires or pins extending through a protective cover. The base contact is made to the N-type germanium die; the two junction contacts (called emitter and collector) are connected to the P-type alloyed regions.

The transistor shown in Figure 1-6 is a power transistor which will amplify, control, and dissipate relatively large amounts of power. These features are a result of the design geometry and the particularly efficient means provided to conduct heat away from the semiconductor junction.

The following chapter describes the physical and electrical characteristics of these versatile devices.

CHAPTER II

Transistor Characteristics . . . Mechanical . . . Electrical Thermal . . . Characteristic Curves . . . Maximum Ratings

2-1 — Mechanical Characteristics

The mechanical characteristics of power transistors are primarily concerned with the physical structure of the device. The single-ended diamond-shaped (TO-3) package was introduced by Motorola in 1955. The straight pins of this package facilitated socket mounting through a heat sink. The TO-3 package has since become one of the industry standards. Sockets generally are not usable with currents of 10 amperes and above due to contact voltage drops and excessive heating losses. The TO-41 package which has the same shape as the TO-3 is available and provides solder lugs for #12 wire to minimize contact losses. A more recent power package, the low silhouette TO-36 supplied by Motorola, is shown in Figure 2-1B.

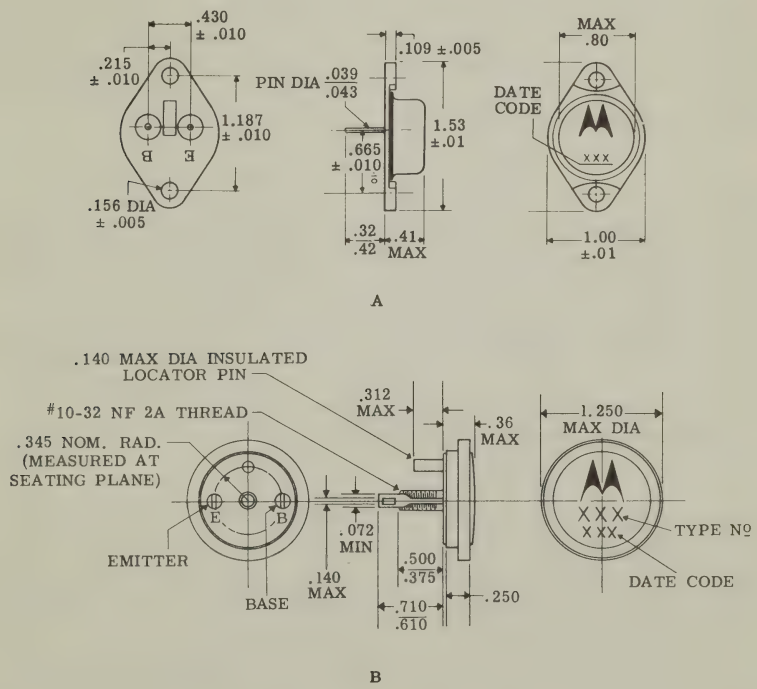


Figure 2-1 — Typical Outline Dimensions

To accomplish heat transfer, Motorola power transistors employ a copper mounting base to which the collector junction is soldered. (This feature will be discussed further under thermal resistance, Section 2-13). Because the collector of the transistor mechanically and electrically contacts the mounting base, the case serves as the collector terminal. The base and emitter pin terminals project through the mounting base and are insulated from it by glass "feed-throughs", which also provide a hermetic seal around the lead. The transistor assembly is completely sealed from external environment by a cap which is either hot or cold welded to the mounting base. While physical appearance may vary with the type of weld employed, the functioning of the seal is the same in either case.

2-2 — Electrical & Thermal Characteristics

To design a circuit, the engineer must take into account the various inherent electrical and thermal characteristics of transistors. A transistor consists of two PN junctions sharing a common, single-crystal base region. Figure 2-2 shows a typical PNP transistor, with the emitter PN junction forward-biased (positive on the emitter) and the collector PN junction reverse-biased (negative on the collector).

As the voltage V_{BE} across the emitter junction is varied, the number of "charge carriers" to the collector also varies. Thus by changing the input voltage, the output current is changed. There are certain basic electrical properties of transistor junctions which account for the relation between input voltage and current and output current and voltage. This relation can be shown by using the classical "black box" (Figure 2-3).

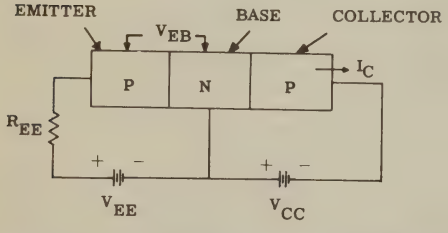


Figure 2-2 — Typical Biasing of PNP Transistor

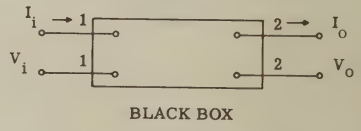


Figure 2-3 — Black Box Equivalent of Transistor

If the transistor is represented as the "black box", then the relationships of the various voltages and currents may be represented by a number of circuit equations. When the output is short-circuited and the input open-circuited, the parameters which relate voltage to current are called "hybrid" or "h" parameters. The "h" parameter equations are:

$$v_1 = h_{11}i_1 + h_{12}v_2, \text{ and} \qquad (2\text{-}1)$$

$$i_2 = h_{21}i_1 + h_{22}v_2. \qquad (2\text{-}2)$$

When $v_2 = 0$ (Short Circuit output),

Then $$h_{11} = \frac{v_1}{i_1}, \text{ and} \tag{2-3}$$

$$h_{21} = \frac{i_2}{i_1}. \tag{2-4}$$

When $i_1 = 0$ (Open Circuit input),

Then $$h_{12} = \frac{v_1}{v_2}, \text{ and} \tag{2-5}$$

$$h_{22} = \frac{i_2}{v_2}. \tag{2-6}$$

The subscript "11" represents the input (i), "21" a forward transfer (f), "12" a reverse transfer (r), and "22" the output (o). Conventional terminology of "h" parameters for small signal conditions is as follows:

Input impedance (ohms) $$h_i = \frac{\partial v_1}{\partial i_1} \tag{2-7}$$

Forward current gain $$h_f = \frac{\partial i_2}{\partial i_1} \tag{2-8}$$

Reverse voltage ratio $$h_r = \frac{\partial v_1}{\partial v_2} \tag{2-9}$$

Output admittance (mhos) $$h_o = \frac{\partial i_2}{\partial v_2} \tag{2-10}$$

The normal mode of operation is common emitter, signified by the addition of subscript "e"; for example, small-signal common-emitter current gain is h_{fe}. Similarly, common base is signified by a "b" subscript, and common collector by a "c". In addition to small signal "h" parameters, large-signal and DC "h" parameters are commonly encountered. All of these are defined in Table 2-1

TABLE 2-1
("h" PARAMETERS FOR COMMON-EMITTER CIRCUIT)

Description	Small Signal	Large Signal	DC
Input Resistance	$h_{ie} = \frac{\partial V_{EB}}{\partial I_B}$	$H_{IE} = \frac{\Delta V_{EB}}{\Delta I_B}$	$h_{IE} = \frac{V_{EB}}{I_B}$
Current Gain	$h_{fe} = \frac{\partial I_C}{\partial I_B}$	$H_{FE} = \frac{\Delta I_C}{\Delta I_B}$	$*h_{FE} = \frac{I'_C - I_{CBO}}{I'_B + I_{CBO}}$

*Where I'_C and I'_B are the values read on a meter.

Since power transistors are usually operated at nearly short-circuit (AC) output, the h_{ie} and h_{fe} parameters are specified and may be used directly for circuit design. Because the input is rarely open-circuited, h_{re} and h_{oe} are seldom specified in data sheets on power transistors.

2-3 — Characteristic Curves

Static or DC curves relating input conditions, transfer functions, and output conditions show how the emitter and collector junctions control the output current. Some typical characteristic curves for Motorola power transistors appear later in this section. The "h" parameters can be obtained from the particular curve representing the same information because they are merely the slope at any point. For example, h_{fe} may be obtained from the I_C vs I_B curve as shown in Figure 2-6.

In addition to the "black box" information, other PN junction characteristics can be represented by a plot of variables. Such things as leakage current and breakdown voltage of the collector are best represented graphically. The effects of temperature on these curves are seen by plotting the curves at several different temperatures. Thus it is possible to completely characterize a transistor by "black box" theory, and voltage, current, and temperature plots. (It will be shown in Section 2-12 that curves also provide a visual description of the maximum ratings of the transistor.) Of course, static curves do not give any frequency information. The frequency cutoff point will be defined in Section 2-5.

2-4 — Special Specifications

End use determines the special Power Gain, Transconductance, and Distortion specifications associated with certain transistors. For example, the Motorola 2N176 Power Transistor was designed for use in the power output stage of automobile radios and hence requires a power gain specification in a specific circuit. Also distortion specification is required for this audio output stage. With switching transistors the important characteristics are DC or large-signal current gain and input resistance. In the latter case however, it is simpler to specify transconductance instead of input resistance. Transistor transconductance is defined as the ratio of collector current to base-emitter voltage, or:

$$g_{FE} = \frac{I_C}{V_{EB}} \qquad \left(\text{note that } g_{FE} = \frac{h_{FE}}{h_{IE}}\right).$$

2-5 — Current Gain Frequency Cutoff

Current gain frequency cutoff ($f_{\alpha e}$) for the common emitter configuration, (also called the beta cutoff frequency) is the frequency where the small-signal, forward-current gain is .707 of the current gain value to be found at a given reference frequency. The .707 point represents a 3 db reduction in current gain. The cutoff frequency is usually between 5kc and 10kc for power transistors. The common base frequency cutoff, $f_{\alpha e}$, (generally not specified for power transistors) is approximately equal to h_{fe} times $f_{\alpha e}$.

2-6 — Switching Characteristics

Switching characteristics involve delay time, rise time, storage time, and fall time. These time periods are derived from a display of the output pulse and

a standard input pulse on an oscilloscope. Figure 2-4 is typical of such a display. In audio switching applications, nonsaturated rise and fall times, t_r and t_f are related to $f_{\alpha e}$ according to the following empirical relations:

$$t_r \times f_{\alpha e} = .3 \quad (2\text{-}11)$$

$$t_f \times f_{\alpha e} = .6 \quad (2\text{-}12)$$

where t_r = nonsaturated rise time, the 10% to 90% points in microseconds,

t_f = nonsaturated fall time, the 10% to 90% points in microseconds, and

$f_{\alpha e}$ = common emitter cutoff frequency, cps.

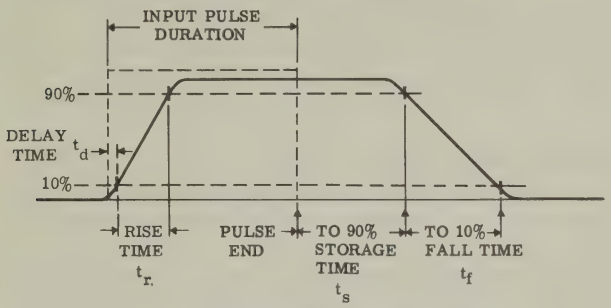


Figure 2-4 — Pulse Response Times

2-7 — Collector Cutoff Current

Collector cutoff current, I_{CBO}, (sometimes shortened to I_{CO}) is the small current that flows from the collector to the base because of the inverse collector potential, which exists when the transistor is cut off. This current is caused by random diffusion of charge carriers across the collector junction, plus leakage currents across the surface of the germanium die that composes the transistor assembly. Every transistor type has a maximum cutoff current value which helps define the range in which it can be used. Typical value of cutoff currents are much less than the maximum value given on data sheets.

I_{CBO} is one of the transistor parameters that is extremely temperature sensitive. Because power transistors generally operate at very high junction temperatures, changes in I_{CBO} at these temperatures can greatly affect stability. The leakage component of I_{CBO} is voltage dependent and therefore the total I_{CBO} is a function of voltage and temperature.

Variation of I_{CBO} with temperature and voltage, for a typical transistor is shown in Figure 2-5. At a given temperature and for a given collector junction area, diffusion (or saturation) component of I_{CBO} varies directly with base resistivity, the greater the resistivity, the greater the diffusion component. Thus this component is larger with higher voltage devices which have higher base resistivity.

2-8 — Emitter Cutoff Current

Emitter cutoff current (I_{EBO}) varies in the same manner as I_{CBO} and the curves are similar.

2-9 — Collector Saturation Voltage

Collector saturation voltage, $V_{CE\ sat}$, (see Figure 2-9) the minimum voltage necessary to sustain normal transistor action at a particular collector current. At this point the emitter-base voltage equals the collector-emitter voltage. At collector voltages lower than $V_{CE\ sat}$ the base-collector diode is forward-biased and the current-voltage relationship changes abruptly. Thus the saturation voltage is the minimum collector-emitter voltage required to maintain full conduction when enough base drive is supplied. Further application of base drive will reduce $V_{CE\ sat}$ with diminishing effect. Since the $V_{CE\ sat}$ vs I_C curve is almost a straight line, some transistor manufacturers list the characteristic as saturation resistance ($r_{CE\ sat}$). $V_{CE\ sat}$ is part of the output characteristic curve as shown in Figure 2-9.

2-10 — Collector Breakdown Voltage

Collector breakdown voltage is the inverse voltage at which the collector junction current begins to avalanche. Under some conditions of operation, especially with inductive loads, the actual voltage appearing at the collector may for a brief time greatly exceed the collector supply voltage, therefore the effects of inductive transients and surges must be taken into consideration. Different types of breakdown voltage characteristics are defined and discussed in Sections 2-16 - 2-20.

2-11 — Power Transistor Characteristic Curves

The important characteristic curves are as follows:

Temperature	Collector cutoff current vs temperature	(Figure 2-5)
Transfer	Collector current vs base current	(Figure 2-6)
Transfer	Collector current vs base-emitter voltage	(Figure 2-7)
Input	Base current vs base-emitter voltage	
Output	Collector current vs collector-to-emitter voltage with base current family	(Figure 2-8) (Figure 2-9)
Output	Collector current vs collector-to-emitter voltage with base-emitter voltage family	
Temperature	Current gain vs collector current and temperature	(Figure 2-10)
Temperature	Transconductance vs collector current and temperature	(Figure 2-11)

Some typical curves for Motorola devices, with an indication of their usefulness, are shown here. The composite curve of Figure 2-12 is an example of how transistor characteristic curves may be used to obtain input to output waveshape relations in a single-ended Class "A" audio amplifier.

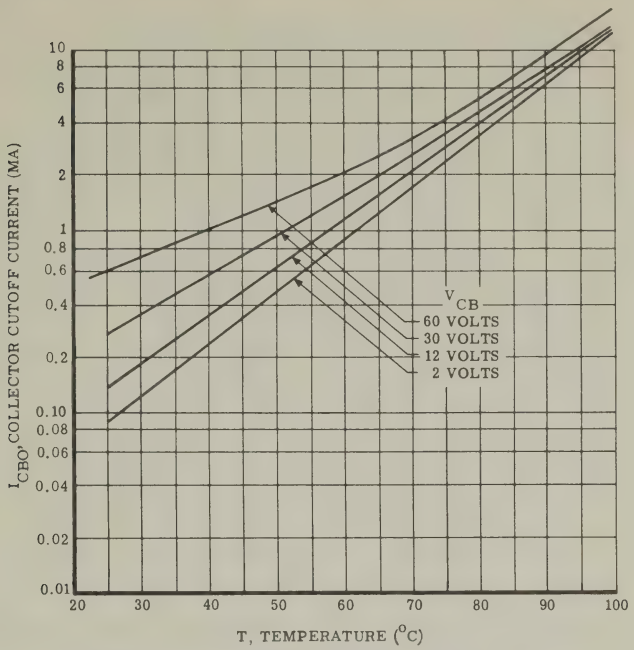


Figure 2-5 — Collector Cutoff Current Versus Collector to Base Voltage and Temperature, 2N1531

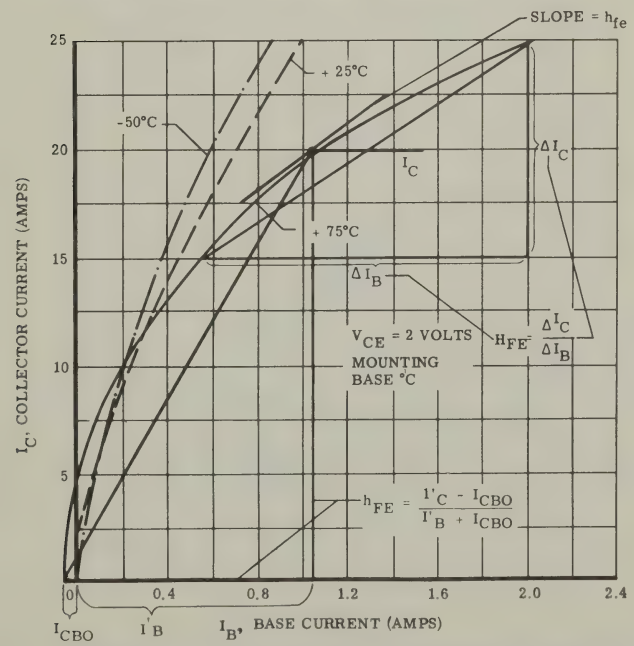


Figure 2-6 — Collector Current Versus Base Current, Motorola 2N1162-1167

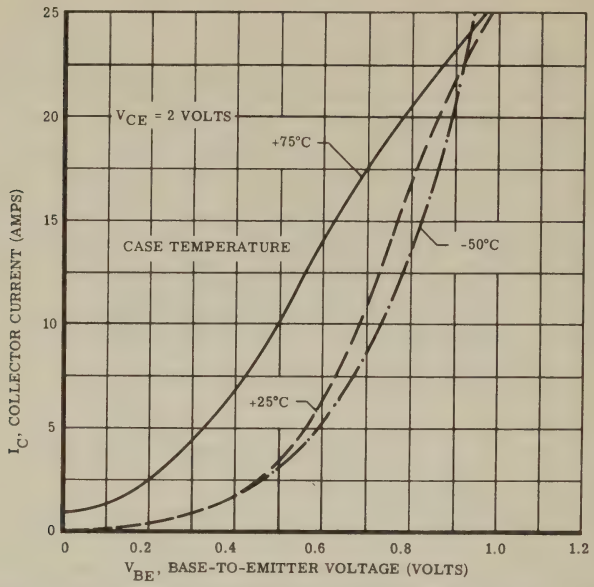


Figure 2-7 — Collector Current Versus Base-to-Emitter Voltage, Motorola 2N1162-1167

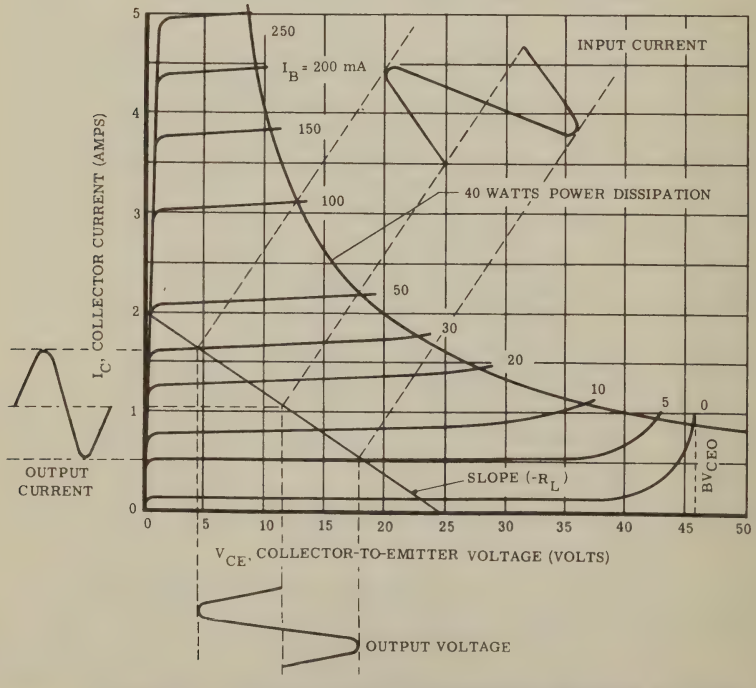


Figure 2-8 — Typical Output Characteristics, Motorola 2N1530

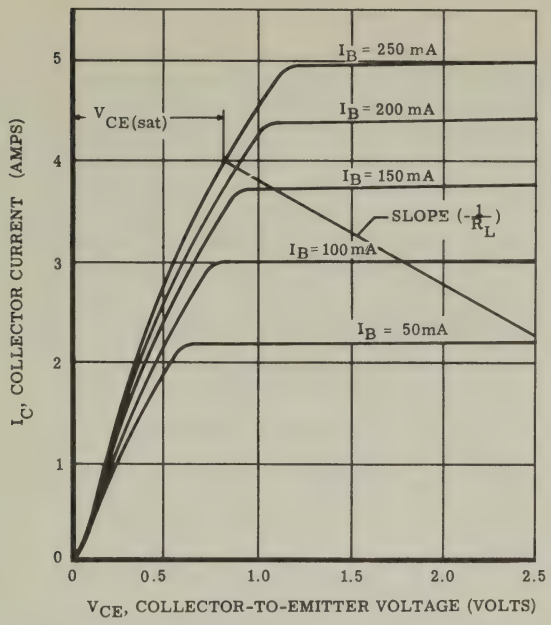


Figure 2-9 — Output Characteristics, Saturation Region, Motorola 2N351A

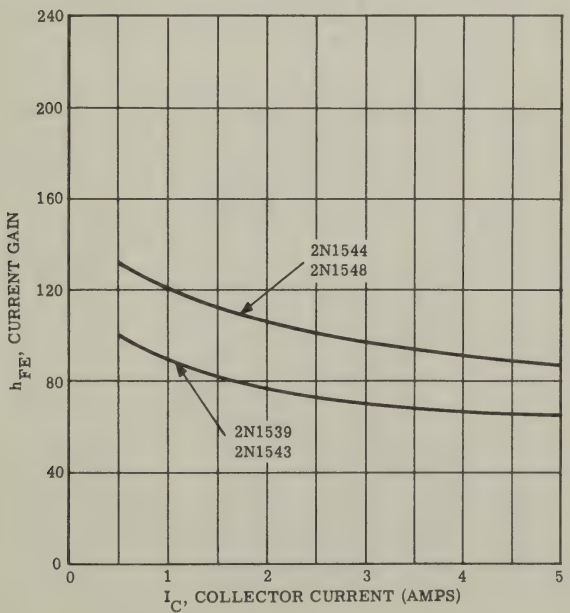


Figure 2-10 — Current Gain Versus Collector Current

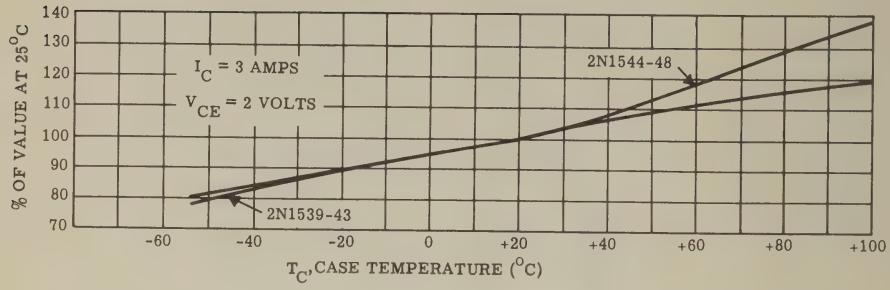
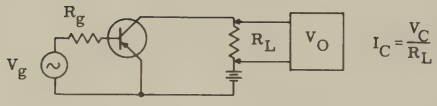


Figure 2-11 — h_{FE} Versus Temperature



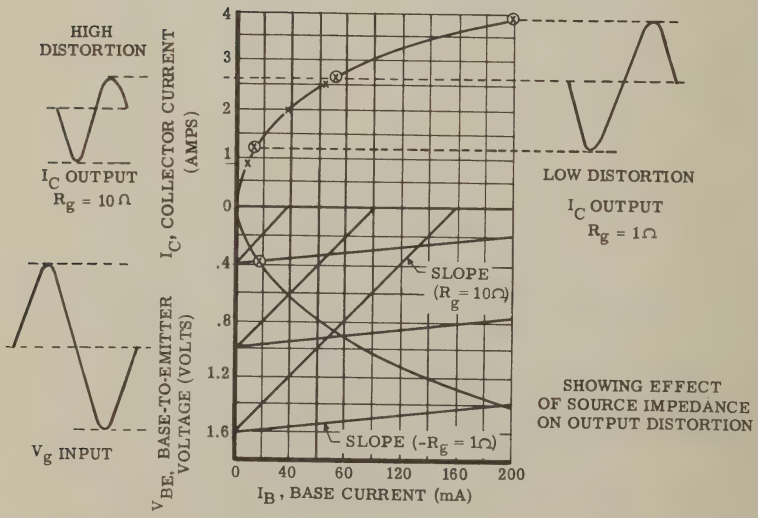


Figure 2-12 — Composite Curve of V_{EB}-I_B and I_C

The input characteristics of a transistor (base-emitter) are also affected by temperature. The manner in which V_{BE} changes with temperature depends on several transistor characteristics. The equivalent input circuit shown in Figure 2-13 will help demonstrate why V_{BE} can have either negative or positive temperature coefficient.

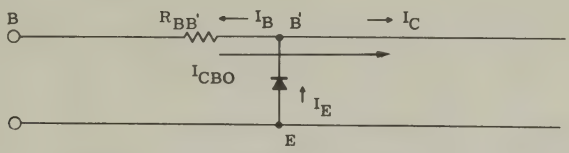


Figure 2-13 — Input Equivalent Circuit

The relations of base-to-emitter voltage, (V_{BE}) can be expressed as:

$$V_{BE} = (I_B - I_{CBO})\ R_{BB'} + V_{B'E}, \text{ or} \qquad (2\text{-}13)$$

$$V_{BE} = \frac{I_C}{h_{FE}} R_{BB'} - I_{CBO}\ R_{BB'} + V_{B'E} \qquad (2\text{-}14)$$

The I_{CBO} function has a positive temperature coefficient whereas the emitter diode voltage ($V_{B'E}$) has a negative one. Both of these reduce V_{BE} as temperature increases, causing the external base-emitter voltage to have a greater negative temperature coefficient than the internal junction ($V_{B'E}$) alone. The current gain term can have positive or negative temperature effects depending on the level of collector current. Thus the term $\frac{I_C}{h_{FE}} R_{BB'}$ can have a positive or negative coefficient. At some current levels the effects can cancel each other and V_{BE} will then be independent of temperature.

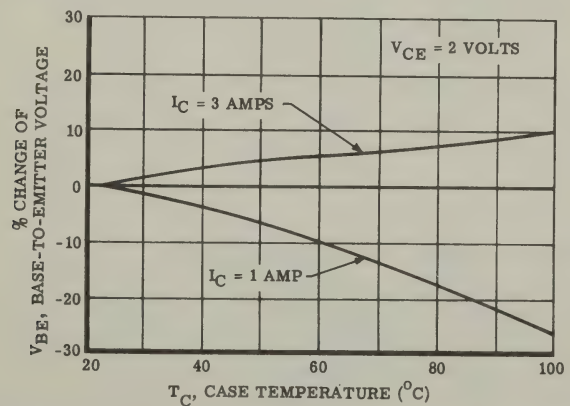


Figure 2-14 — Percent Change of Base-to-Emitter Voltage Versus Mounting Base Temperature, Motorola 2N375

The V_{BE} vs temperature curve for the Motorola 2N375 transistor is shown in Figure 2-14. Note that somewhere between $I_C = 1$ and 3 amps, V_{BE} is constant. If the V_{BE} vs temperature curve is a reasonably straight line, the V_{BE} temperature coefficient can be plotted as in Figure 2-15.

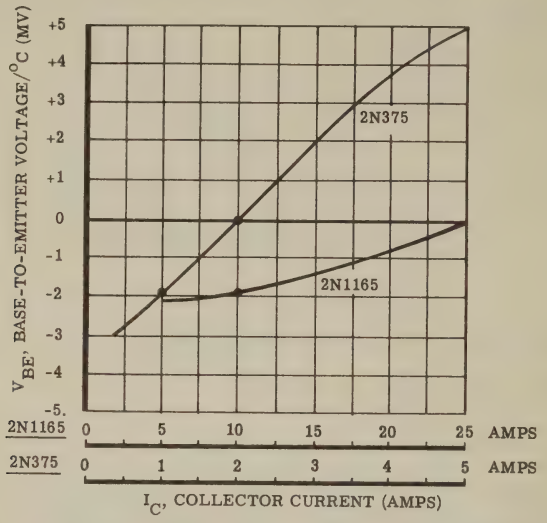


Figure 2-15 — Base-to-Emitter Voltage Change Versus Collector Current, Motorola 2N375, 2N1165

2-12 — Maximum Ratings

There are generally four maximum ratings given to a power transistor. These are:

1. Maximum power dissipation
2. Maximum collector junction temperature
3. Maximum collector current
4. Maximum collector voltage

Ratings 1 and 2 are related by the thermal characteristics of the device. Ratings 3 and 4 form a zone of reliable $V_C - I_C$ operating areas. The following sections describe in detail operation characteristics within these maximum ratings.

2-13 — Maximum Power and Temperature

Maximum power and junction temperature are related since junction temperature rise is caused by power dissipation. The maximum allowable junction temperature is 100°C for Motorola germanium power transistors. This 100°C rating is based upon long term continuous operation at this temperature. Production life tests are made with the transistor held at 100°C for 500 to 1,000 hours and even longer time periods. Only a slight degradation in performance is allowed at the end of this test. For shorter intervals of time it is obvious that

the transistor will withstand temperatures higher than 100°C. One of the limitations is the melting point of indium which is 156°C. There is also a slight softening of the junction at approximately 125°C.

The average power dissipation may be approximated as:

$$P_D = I_E V_{CE} \tag{2-15}$$

For a given power level this equation will plot as a hyperbolic curve as illustrated in Figure 2-8. The power dissipation is related to junction temperature by a thermal coefficient which is usually called thermal resistance. The term thermal resistance arises from converting heat effects to an equivalent electrical analogy. In the analogy, the following conversions exist:

Thermal	Symbol	Units	Electrical
Power Dissipation	P_D	Watts	Constant current generation
Temperature Rise	ΔT	°C	Voltage rise
Thermal Resistance	θ	°C/W	Resistance
Thermal Capacitance (Specific heat)	C	W-sec/°C	Capacitance

In the steady state case, the equivalent circuit will be as detailed in Figure 2-16.

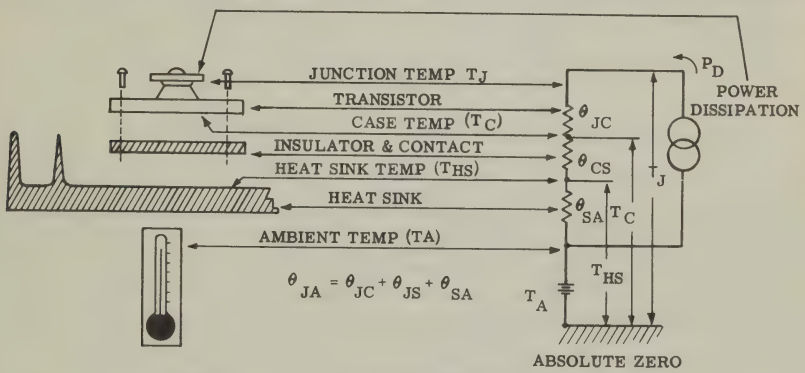


Figure 2-16 — Thermal-to-Electrical Analogy

The equivalent electrical circuit yields to Kirchoff's Law and the following equations result:

$$T_J = P_D \theta_{JC} + P_D \theta_{CS} + P_D \theta_{SA} + T_A \tag{2-16}$$

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A \tag{2-17}$$

$$\text{Let } \theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \tag{2-18}$$

where θ_{JA} is total thermal resistance (junction to ambient)

θ_{JC} is transistor thermal resistance (junction to case)

θ_{CS} is insulator thermal resistance (case to heat sink)

θ_{SA} is heat sink thermal resistance (heat sink to ambient)

then $$T_J = P_D \theta_{JA} + T_A \tag{2-19}$$

(Note that the junction temperature "floats" upon the ambient temperature)

The thermal resistance of the transistor is the sum of the thermal resistances in the heat conduction path from collector junction to the surface of the mounting base. Motorola industrial power transistors in the TO-3 case have 0.8°C/W maximum thermal resistance or less. The automotive power units are designed with a thermal resistance of 1.2°C/W maximum. The maximum power and temperature ratings of the transistor may be represented by a derating curve as shown in Figure 2-17 where the solid line is a negative derating slope equal to transistor thermal resistance (θ_{JC}).

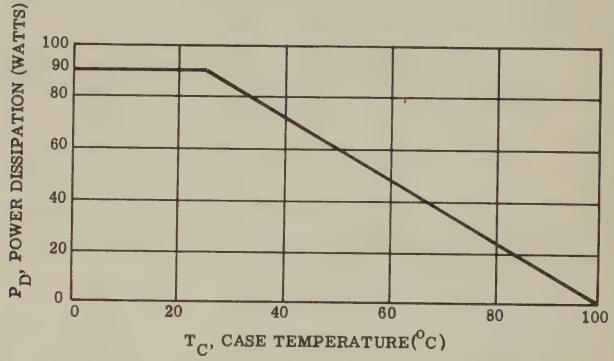


Figure 2-17 — Power-Temperature Derating Curve

In the practical situation the ambient temperature is the uncontrolled variable and the junction temperature must be controlled by the thermal resistance of the heat sink. The heat sink thermal resistance is dependent upon the type of material (usually aluminum), shape, thickness, color, area, temperature and air flow. The minimum value of θ_{SA} may be calculated from the following equation:

$$\theta_{SA} = \frac{T_{J\,max} - T_A}{P_D} - \theta_{CS} - \theta_{JC} \qquad (2\text{-}20)$$

As an example:

$P_D = 10$ watts (total dissipation)

$\theta_{JS} = 0.6$°C/W (mica insulator)

$\theta_{JC} = 0.8$°C/W (industrial power transistor)

$T_{J\,max} = 100$°C

$T_A = 50$°C

$$\theta_{SA} = \frac{100 - 50}{10} - .6 - .8 = 3.6\text{°C/W}.$$

Motorola provides a heat sink, Type MS-10, which would be applicable to this example. It has a $\theta_{SA} = 2.75$°C/W at the 10 watt level. The MS-10 heat sink is illustrated in Figure 2-18.

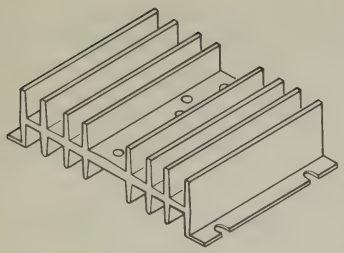


Figure 2-18 — Transistor Heat Sink MS-10

The most convenient and satisfactory way to mount the Motorola power transistors to the heat sink is with a Motorola Mounting Kit MK-10, MK-15, or MK-20. These kits provide a high-quality power transistor socket, mounting screws, a transistor insulating washer, drilling template and mounting instructions. Table 2-2 lists the various kits and the thermal resistance (θ_{CS}) of the insulators.

TABLE 2-2 MOTOROLA MOUNTING KITS

Kit No.	Insulating Washer	Typical Mounting Thermal Resistance (Θ_{CS}) °C/W (includes contact resistance)	
		Dry	With DC4*
——	No insulator	.62	.41
MK-10	Teflon	1.45	.80
MK-15	Mica	1.35	.60
MK-20	Anodized Aluminum	1.20	.75

*DC4 is Dow Corning No. 4 Silicone Lubricant. The use of the DC4 or equivalent is highly recommended especially for high power applications. The grease should be applied in a thin layer on both sides of the washer. When transistors are replaced in the sockets a new layer of the grease should be added.

The teflon insulator is very durable and heat resistant but is somewhat inferior in heat conductivity and is not as strong mechanically as the mica and aluminum insulator.

The mica and anodized aluminum washers are recommended for good thermal conduction. However, mica is subject to flaking and cracking and the anodized aluminum to scratching or denting. Scratching of both sides may result in penetration of the thin insulating layer with consequent electrical shorting.

An exploded view of the mounting method using these kits is given in Figure 2-19.

Power transistors which are equipped with solder lugs on the pins cannot be used with the standard sockets. These may be mounted to a heat sink by bolting directly to the metal, or by using any of the insulating washers recommended in the mounting kits. When insulating washers are used, the bolts also must be insulated from either the transistor case or the heat sink. This may be accomplished by using a suitable fibre shoulder washer. An alternative method is to insulate the individual heat sinks.

A nomograph which relates allowable power dissipation to ambient temperature when using the MS-10 and the Motorola mounting kits is given in Figure 2-20. An example of how the nomograph is used follows.

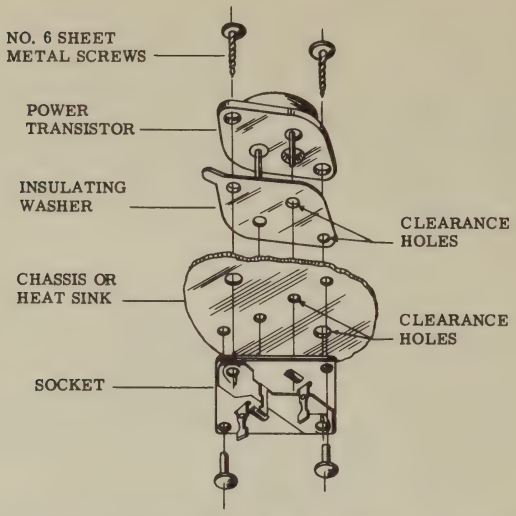


Figure 2-19 — Method of Mounting Motorola Power Transistors

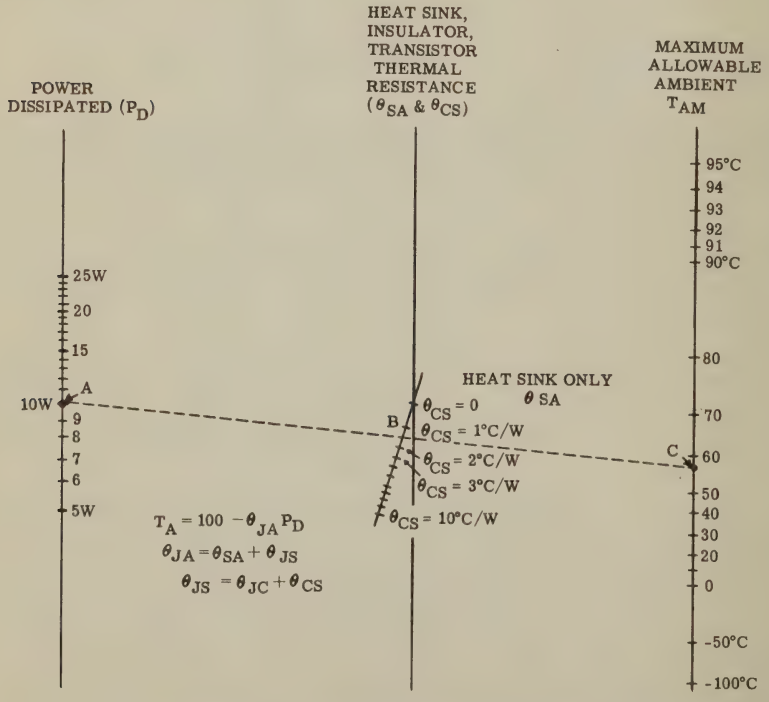


Figure 2-20 — Nomograph For Motorola Heat Sink MS-10
(Allowable Power Dissipation Versus Ambient Temperature)

Problem: What maximum ambient temperature is allowed when the following conditions are true:

$P_D = 10$ watts

$\theta_{CS} = 0.6°C/W$ (MK-15 insulator kit)

$\theta_{JC} = 0.8°C/W$

$\theta_{JS} = \theta_{JC} + \theta_{CS} = 1.4°C/W$

Solution:

(Refer to Figure 2-20)

1—Set 10 watts on nomograph (Point A on power scale)

2—Set $\theta_{JS} = 1.4°C/W$ (Point B on thermal resistance scale)

3—Connect Points A and B with a straight line extending to temperature scale.

4—Read maximum allowable $T_A = 58°C$ at Point C.

The entire problem of temperature and power limits may be generalized for any heat sink as shown in the nomograph of Figure 2-22. Scale E of the general nomograph indicates total heat sink area for flat square sheets of ⅛" bright aluminum. Thermal resistance of these sheets plotted against the total area (both sides) is shown in Figure 2-21.

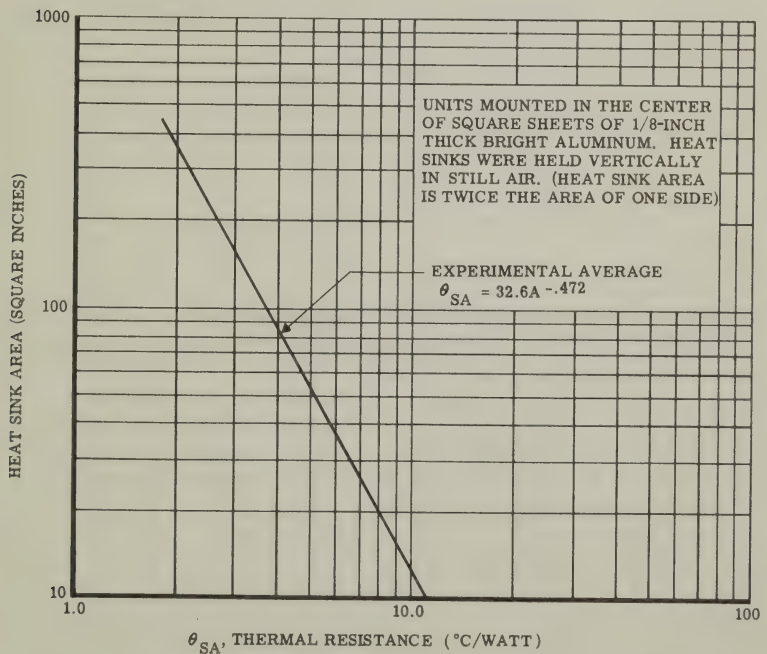


Figure 2-21 — Heat Sink Area Versus Thermal Resistance

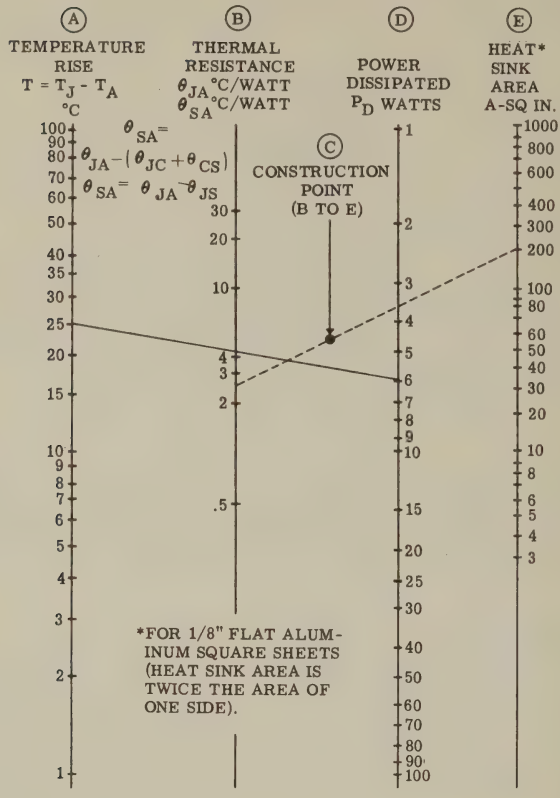


Figure 2-22 — General Heat Sink Nomograph

An example of the general nomograph is as follows.

Problem: What heat sink thermal resistance, θ_{SA}, and area is required when

$$T_{j\,max} = 100°C$$
$$T_A = 75°C$$
$$P_D = 6 \text{ watts (total)}$$
$$\theta_{JC} = 0.8°C/W$$
$$\theta_{CS} = 0.6°C/W$$
$$\theta_{JS} = \theta_{JC} + \theta_{CS} = 1.4°C/W$$

Solution:

(Refer to Figure 2-22)

1—$T_J - T_A = 25°C$; enter scale A at 25°C.

2—Enter Scale D at 6 watts.
3—Join 25°C and 6 watts with a straight line intersecting line B.
4—Read 0 = 4.1°C/W (total thermal resistance, θ_{JA}) on Scale B.
5—Obtain θ_{SA} (heat sink thermal resistance) mathematically; $\theta_{SA} = \theta_{JA} - \theta_{JS}$, or $\theta_{SA} = 4.1 - 1.4 = 2.7$°C/W.
6—Enter line B at 2.7°C/W and construct a line from this point through the construction point C extending to E.
7—Read 200 sq. in. This would be 100 sq. in. per side or a flat square sheet ⅛" × 10" × 10".

The temperature control methods which have been described are general. When designed with heat sinks, the mounting base temperature of the transistor should be monitored with a thermocouple under the worst foreseeable conditions. The many factors which determine the ability of a heat sink to transfer heat into the ambient makes this precaution vital.

2-14 — Pulse Power Dissipation Effects

Pulse power dissipation effects depend on the thermal capacitance of the device as well as the thermal resistance. The two generally are considered as a parallel R-C network. The effects can be expressed as a thermal time constant which is the product of resistance and capacitance, $\tau_{JC} = \theta_{JC} \times C_{JC}$ (in seconds).

This time constant is defined as the time in seconds required for the junction temperature to rise to 63% of its final value. Power surges must be limited so that junction temperature does not go above the maximum limit rating of 100°C.

Consider the example where repetitive power pulses (P_P) are being handled by the transistor. If an infinite heat sink is used such that the case temperature equals ambient temperature, the temperature rise may be shown to be:

$$\Delta T = T_J - T_C = P_P \theta_{JC} \left[\frac{1 - e^{-t_1/\tau_{JC}}}{1 - e^{-t/\tau_{JC}}} \right] \qquad (2\text{-}21)$$

The repetition rate (frequency is the inverse of the period t, or F = 1/t. The pulse width is shown as t_1. The duty cycle will be defined as the ratio of pulse width to the period in percent, or duty cycle = (t_1/t) 100%. The junction temperature will rise less as the duty cycle and pulse width decrease. Of course, the pulse shape must be considered as a perfect rectangle as shown in Figure 2-23. When the repetition rate is in excess of about 5 kc, rise, fall, and storage times will effectively widen the pulse duration. These effects also will increase the duty cycle and less maximum pulse power can be tolerated.

Equation 2-21 was derived by a mathematical analysis of the thermal network, assuming that the power pulses are the equivalent of a constant-current generator feeding a parallel R-C network. Essentially the thermal network integrates the power pulses, resulting in a temperature rise in the junction.

If the expression inside the bracket of Equation 2-21 is designated $1/C_{PJC}$, the term C_{PJC}, or coefficient of power of the transistor can be plotted as a function of pulse width and duty cycle for a thermal time constant of 50 ms as shown in Figure 2-24.

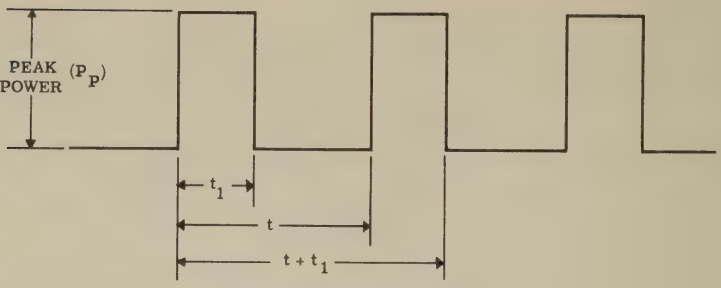


Figure 2-23 — Power Pulses

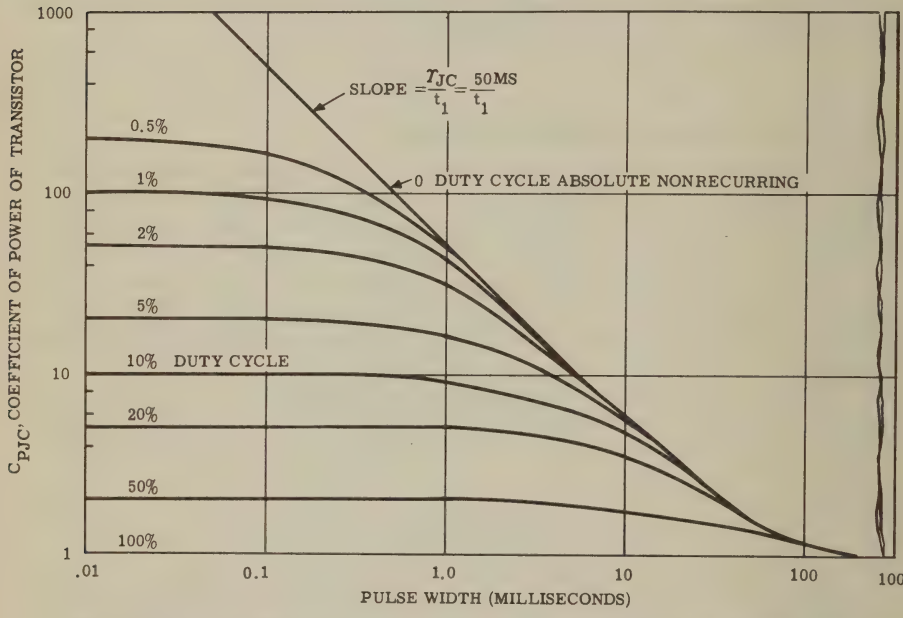


Figure 2-24 — Coefficient of Peak Power Versus Pulse Width and Duty Cycle

The peak allowable power (P_P) may be determined by rearranging Equation 2-21 and using the chart of Figure 2-24.

Infinite Heat Sink Situation:

$$P_P = \left(\frac{T_{J\,max} - T_C}{\theta_{JC}}\right) C_{PJC} \qquad (2\text{-}22)$$

For instance, for Motorola industrial power transistors in the diamond TO-3 package $T_{J\,max} = 100°C$, $\theta_{JC} = 0.8°C/W$, and, at $T_C = 25°C$,

$$P_P = 90\ C_{PJC} \qquad (2\text{-}23)$$

In a practical situation the heat sink will be finite and a finite thermal resistance between ambient and the case will add to the internal thermal resist-

ance. However, most heat sinks will have very large thermal capacitances as compared to that of the transistor. A heat sink "coefficient of power," C_{PCA} can be found by plotting the bracketed term of Equation 2-21 as a function of pulse width, duty cycle, and the thermal time constant, τ_{CA}, of the heat sink. The power pulses will then cause a rise of case temperature on the basis of the heat sink "coefficient of power," or,

For a Finite Heat Sink:

$$T_C = T_A + \frac{P_P \theta_{CA}}{C_{PCA}} . \tag{2-24}$$

The peak allowable power for a finite heat sink is:

$$P_P = \frac{T_J - T_A}{\frac{\theta_{JC}}{C_{PJC}} + \frac{\theta_{CA}}{C_{PCA}}} \tag{2-25}$$

Frequently the pulse width will be very short compared to the heat sink thermal time constant and the value of C_{PCA} may be approximated by (t/t_1). For nonrepetitive pulses $C_{PCA} = \tau_{CA}/t_1$. That these approximations are true may be determined by expanding the exponential terms of Equation 2-21 into an infinite series and allowing the time constant (τ) to approach infinity in the first case, and in the second case allow the period (t) to approach infinity.

When $\theta_{CA} = 0$ (infinite heat sink), Equation 2-25 is identical to Equation 2-22. Both equations have assumed no steady state power except in the one limit where the pulse width is much longer than the transistor time constant. Generally there will be a certain amount of steady power. Upon this steady state power the peak pulses will be superimposed. Obviously the peak allowable power will be diminished when steady state power is present. Steady state power (P_{SS}) causes a certain level of junction temperature when no pulse power is present, and can be represented as an increase in ambient temperature when considering allowable peak power. The following is the general peak allowable power formula:

$$P_P = \frac{T_J - T_A - \theta_{JA} P_{SS}}{\frac{\theta_{JC}}{C_{PJC}} + \frac{\theta_{CA}}{C_{PCA}}} . \tag{2-26}$$

Two examples involving peak allowable power will be presented to more fully explain the use of the preceding expressions and the normalized chart of Figure 2-24.

Example Number 1

Given:

1—Ambient Temperature, $T_A = 70°C$.
2—Steady State Power, $P_{SS} = 0$.
3—Pulse width, $t_1 = 2$ millisec.
4—Period, $t = 10$ millisec.
5—Heat Sink plus interface, $\theta_{CA} = 3°C/W$.
6—Heat Sink time constant $\tau_{CA} = 500$ millisec.

Problem:

What is the allowable peak power with a 90 watt Motorola Industrial Power Transistor?

Solution:

1—Duty Cycle, $\frac{t_1}{t} = \frac{2}{10} = .2$ or 20%; hence $C_{PCA} = 5$

2—Enter chart of Figure 2-24 at $t_1 = 2$ millisec and 20% Duty Cycle. Read $C_{PJC} = 4$.

3—Calculate P_P from Equation 2-25. $P_P = \frac{100 - 70}{\frac{0.8}{4} + \frac{3}{5}} = 37.5$ watts.

Notice in this example the pulse width was short compared to the thermal time constant and an approximation based on duty cycle alone would give 40 watts allowable.

Example Number 2:

Given: A DC to AC inverter with the following conditions:

1—Ambient Temperature (T_A) = 50°

2—Frequency = 500 CPS

However there are two power pulses per cycle during switching and the effective Period, t, = 1 millisec.

3—Switching time (t_1) = 10μsec, (Rise and Fall are equal).

4—Duty cycle (t_1/t) = 1%.

5—Peak collector current ($I_{C\,max}$) = 10A.

6—Peak collector voltage ($V_{CE\,max}$) = 60V.

7—Transistor Thermal resistance (θ_{JC}) = 0.8°C/W.

8—External Thermal resistance (θ_{CA}) = 1.7°C/W.

9—External thermal time constant (τ_{CA}) = 500 millisec.

10—Maximum allowable junction temperature ($T_{J\,max}$) = 100°C.

Problem:

Will the allowable $T_{J\,max}$ of 100°C be exceeded?

Solution:

If the peak power plus steady state power is less than the calculated allowable power then $T_j < 100$°C. Actual Peak power dissipated $P_D = \frac{V_{CE\,max}}{2} \times \frac{I_{C\,max}}{2} = 30 \times 5 = 150$w (assuming a straight line switching load).

Calculate allowable power from Equation 2-26.

Where C_P from the 1% duty cycle line of Figure 2-24 is 100; also C_{PCA} is 100:

Solution:

$$P_P = \frac{100 - 50 - 2.5 \times 2}{\frac{0.8}{100} + \frac{1.7}{100}}$$

$P_P \approx 1800$ watts

Since the actual peak power (150w) is less than the allowable power (1800w) $T_{J\ max}$ will not exceed 100°C.

Caution — — — The peak allowable power is based strictly upon temperature rise. Many times this value will be beyond the safe voltage and current limits of the transistor, as defined in the next Section. *Both safe areas and allowable power limits must be observed.*

2-15 — Maximum Voltage and Current in Power Transistors

In alloyed germanium PNP power transistors there exist definite areas for reliable operation with regard to collector voltage and collector current. Typical areas are shown in Figure 2-25. In this figure the term "maximum reliability area" means that as long as the collector load line is within this area the transistor will not short out. The dotted area is bounded on the outer side by the "absolute maximum limit" line which must not be exceeded, since a collector-to-emitter short may result. The cross-hatched area can be considered as a "derated" zone of operation which provides the designer with a safeguard insofar as unknown or occasional power surges are concerned. On the other hand, when operating in the dotted area, the designer must be absolutely certain that no power surge will occur that might cause the operating point to cross over the maximum limit. It is only necessary for the collector load line to penetrate the "unsafe" area for a few microseconds to trigger a short. This short is induced by what is called "second breakdown", which is discussed in more detail at the end of this chapter.

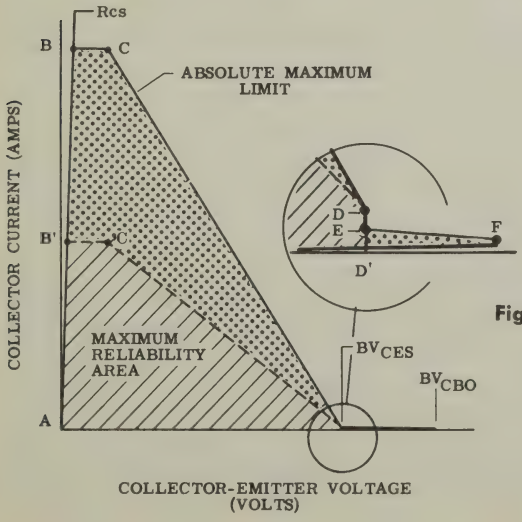


Figure 2-25 — Reliable V_C-I_C Areas

In general, it is permissible to switch through high power dissipation areas if the switching is rapid. The reason for this is that the junction temperature, which must also be considered, is dependent on the average power dissipation rather than the maximum power dissipation. The characteristics numbered on the graph, Figure 2-26, are commonly used test conditions and also cover most of the common operating conditions.

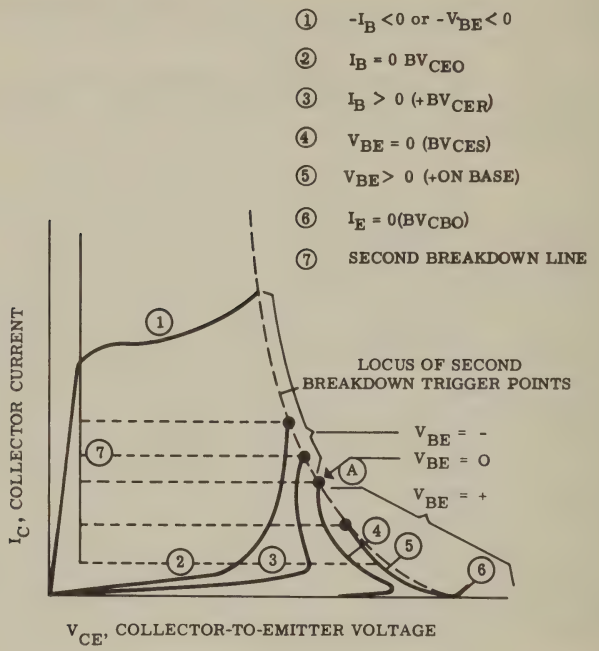
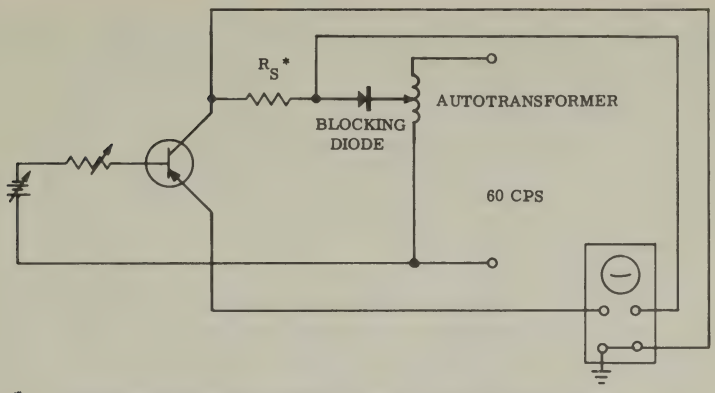


Figure 2-26 — Collector Current Versus Collector-to-Emitter Voltage

Line 1: Base current held constant at some negative value. This is the most common mode of operation. A constant base-emitter voltage, negative on the base, would show a similar curve.
Line 2: Base current equal to zero. (Commonly called $\alpha m = 1$ curve)
Line 3: Base current held constant to some positive value.
Line 4: Base emitter voltage equal to zero.
Line 5: Base-emitter voltage held constant with positive voltage on the base.
Line 6: Emitter open. Corresponds to collector-base breakdown characteristic or the I_{CBO} line.
Line 7: Characteristic trace after second breakdown had been triggered.

A test set-up to observe transistor characteristics is shown in Figure 2-27. The oscilloscope used should have a bandpass of several megacycles. All of the numbered lines shown result while subjecting the base-emitter junction to the indicated condition and increasing the voltage across the collector base junction.



*R_S, THE CURRENT SENSING RESISTOR, SHOULD BE NONINDUCTIVE

Figure 2-27 — Typical Breakdown Voltage Characteristic Test Display

Line 2 is often called BV_{CEO}, V $_{\alpha}$m, or $_{\alpha}m = 1$. It is the curve which would be generated by opening the base. Line 3 has been named BV_{CER}, indicating that this is the breakdown curve when there is a resistance between base and emitter. Line 4 is generally called BV_{CES}, V_{CEB}, or "first breakdown", a non-destructive condition. Lines 3, 4 and 5 usually have a negative resistance portion beginning at a high voltage and low current (from 1-50mA) and falling back to a lower voltage and higher current (100-500 mA) before going into avalanche. Line 5 is called BV_{CEX}. Line 6 is the path of collector cutoff current (I_{CBO}), and the point where the current begins to avalanche is called collector-to-base breakdown (BV_{CBO}) or "Diode Avalanche".

The shape of the lines is determined by the physical construction of the transistor and the materials used. Such things as base resistivity, base width, surface conditions of the germanium, collector cutoff current (I_{CBO}) and avalanche multiplication are all determinants of line shape. The references at the end of the Chapter all have excellent sections discussing the relation of transistor characteristics to breakdown. There is also a brief discussion of this relation in the Appendix of the Chapter.

2-16 — Second Breakdown Voltage

Second Breakdown Voltage, a destructive condition, was first observed when the first breakdown condition ($V_{BE} = 0$) was allowed to continue until point "A" was reached as illustrated by line 4 (BV_{CES}) of Figure 2-26. The current was allowed to increase after the curve had entered into the first negative resistance portion and a second negative resistance occurred which switched the characteristic onto Line 7 of Figure 2-26. Further investigation has shown that other base-emitter conditions trigger second breakdown. If the base-shorted-to-the-emitter ($V_{BE} = 0$) condition is used as a reference point, there exists a locus of points where second breakdown is initiated for both negative and positive base-to-emitter voltage conditions which is shown by the dashed line. Thus, high negative base drive will cause second breakdown to be generated at much

greater collector current by a lower collector voltage than at the $V_{BE} = 0$ point. When the base is positive the locus is more difficult to determine since the trigger point lies in a negative resistance region. The exact locus varies considerably from one device to the next. However, if the collector diode breakdown and the BV_{CES} are within specifications for the transistor, the locus will always be to the right of and above lines D-E and E-F of Figure 2-25. Triggering second breakdown from positive base drive almost always results in a collector-to-emitter short or a drastically altered transistor. Negative drive action does not appear to be as drastic and usually the phenomenon can be observed repeatedly on an oscilloscope curve tracer.

The exact physical reaction is still somewhat of a mystery, although the results of other types of breakdown have been fully described. Second breakdown seems to result in a "channeling of current" between the collector and emitter. In second breakdown the collector-to-base junction exhibits certain instabilities when high voltage is applied. The point at which these instabilities occur is controlled by the voltage imposed on the base-to-emitter junction. This spot heating can actually melt the germanium and allow the indium of the collector and the emitter to flow together producing a collector-emitter short.

The locus of points where second breakdown occurs is independent of temperature within normal operating ranges. However as temperature changes, a particular point on the locus will shift with a certain base-emitter condition. For instance, as temperature increases, the $V_{BE} = 0$ point will shift toward the $I_B = 0$ line. This is because more I_{CBO} flows through the internal base resistance ($R_{BB'}$) which causes the internal base-emitter junction to see a more negative voltage on the base side. In fact, high I_{CBO} current will cause the $V_{BE} = 0$ line to lose its negative resistance portion (the tail) and approach the low temperature $I_B = 0$ case.

A back bias voltage just equal to the $I_{CBO} \times R_{BB'}$ product would cancel out this effect and its output characteristic line would follow the temperature $V_{BE} = 0$ curve. Thus the basic "reliable" and "absolute maximum" lines are independent of temperature but load lines may shift with temperature.

Safe areas are assured by Motorola for a specific transistor by the following tests: (Refer to Figures 2-25 and 2-26)

TABLE 2-3
BASIC TESTS USED BY MOTOROLA TO ASSURE RELIABILITY

1. BV_{CES} is measured at or to the right of Point D (generally the transistor is given a curve tracer test which sweeps it beyond this point). This is the basic test to assure the maximum collector-to-emitter voltage rating.
2. I_{CBO} is measured at or above Point F.
3. Points C and E are determined by sampling tests.
4. Point B is based upon either minimum usable low voltage current gain or upon the collector saturation voltage.

(Note that the area above line BC, while not necessarily unreliable, may involve the use of current gain that is too low for practical considerations or may be above the current handling capabilities of the emitter pin.)

Thus, there exists a high reliability safe area AB'C'DED'A and two probably safe areas B'BCDC'B' and D'EFD'. Specific operating areas for Motorola's power transistors are shown in the last section of this Chapter.

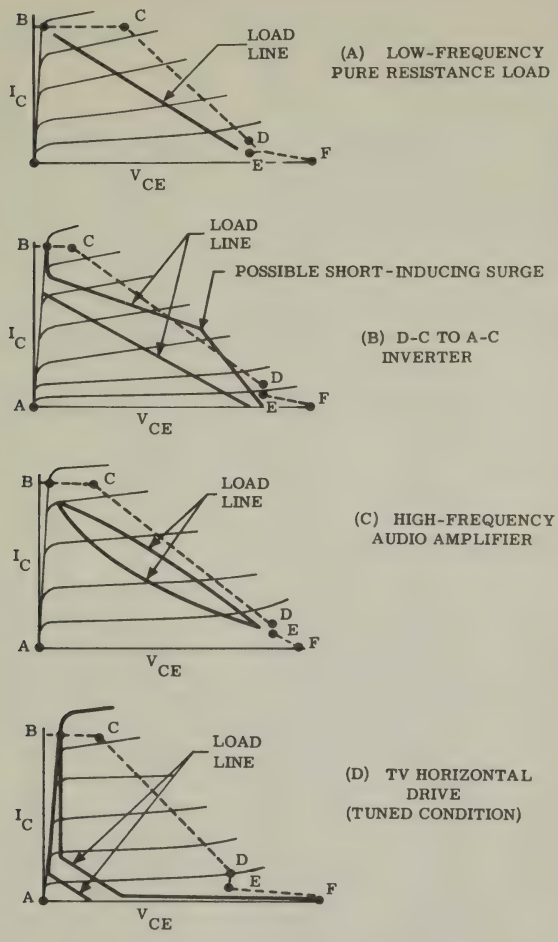
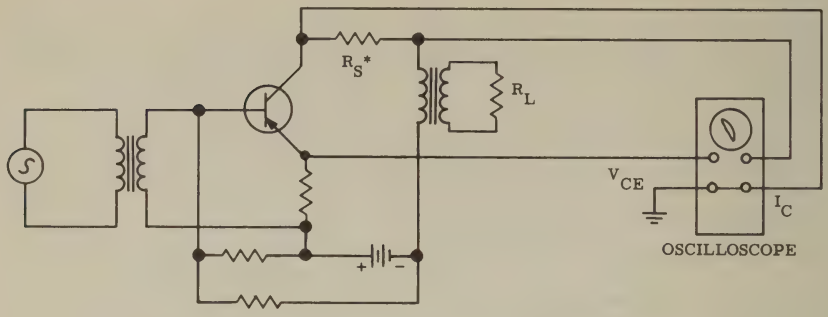


Figure 2-28 — Typical Load Lines

2-17 — Load Line Analysis

Generally the circuit variations which may affect the shape of a particular load line cannot be rigorously analyzed. All circuits should be checked with an oscilloscope to determine what areas the load line circumscribes. If possible the test should be run over the entire operating temperature range. A test set-up to observe the load line is indicated in Figure 2-29. The load line of an audio amplifier can be observed by inserting a sampling resistance, as small as practical, in the collector lead and observing the collector current with an oscilloscope as shown in Figure 2-29

The oscilloscope used for load line testing should have a bandpass of several megacycles. Some typical load lines are shown in Figure 2-28.



*R_S, THE CURRENT SENSING-RESISTOR, SHOULD BE NONINDUCTIVE

Figure 2-29 — Typical Audio Amplifier Load Line Analysis Setup

2-18 — Punch-Through Voltage

Another voltage phenomenon unique to transistors is termed "punch-through" voltage. This phenomenon can be explained in terms of base width and base resistivity. As reverse voltage is increased across the collector to base diode, the space charge region or depletion layer at the junction increases in width. Most of the increase takes place in the base region, moving towards the emitter junction. This increase varies as the base resistivity. Since the effective base width is from the edge of the emitter space charge zone to the edge of the collector space charge zone, the base width will decrease as the collector edge advances toward the emitter. At some collector voltages the collector space charge zone will reduce the base width to zero and the emitter will be electrically shorted to the collector. The voltage required to do this is called "punch-through" voltage.

Punch-through does not damage the transistor if current is limited, although transistor action is temporarily disrupted. Once the voltage is removed normal action is resumed. Although Motorola does not specify a punch-through characteristic, every power transistor is given a punch-through test during the manufacturing process.

This test is assurance that each transistor has a "punch-through" voltage equal to or in excess of the collector diode breakdown (BV_{CBO}).

2-19 — Specific Reliability Areas

The general "high reliability" and "absolute maximum" lines for Motorola power transistor are listed in table 2-4. The table listings indicate the value of current and voltage for a specific transistor at each point of the general curve of Figure 2-25.

TABLE 2-4 *(See Figure 2-25)*
SPECIFIC RELIABILITY AREAS FOR MOTOROLA TRANSISTORS

	B	C	D	E	F(BV_{CBO})	G*
	$V_{CE\ sat}$ at I_C of		(BV_{CES})		I_{CBO} at V_{CB} of	
2N176	3A	25V, 3A	30V, .3A	30V,.1A	40V	—
2N350A	3A	35V, 3A	40V, .5A	40V,.1A	50V	—
2N351A	4A	32.5V,4A	40V, .5A	40V,.1A	50V	—
2N375	5A	40V, 5A	60V, .5A	60V,.1A	80V	—
2N376A	5A	30V, 5A	40V, .5A	40V,.1A	50V	—
2N618	5A	40V, 5A	60V, .5A	30V,.1A	80V	—
2N627	10A	20V, 10A	30V, .5A	30V,.1A	40V	—
2N628	10A	25V, 10A	45V, .5A	45V,.1A	60V	—
2N629	10A	30V, 10A	60V, .5A	60V,.1A	80V	45V,4A
2N630	10A	35V, 10A	75V, .5A	75V,.1A	100V	50V,4A
2N669	3A	25V, 3A	30V, .3A	30V,.1A	40V	—
2N1162	25A	20V, 25A	35V,1.0A	35V,.1A	50V	—
2N1163	25A	20V, 25A	35V,1.0A	35V,.1A	50V	—
2N1164	25A	20V, 25A	60V,1.0A	60V,.1A	80V	—
2N1165	25A	20V, 25A	60V,1.0A	60V,.1A	80V	—
2N1166	25A	20V, 25A	75V,1.0A	75V,.1A	100V	—
2N1167	25A	20V, 25A	75V,1.0A	75V,.1A	100V	—
2N1359	5A	30V, 5A	40V, .5A	40V,.1A	50V	—
2N1360	5A	30V, 5A	40V, .5A	40V,.1A	50V	—
2N1362	5A	50V, 5A	75V, .5A	75V,.1A	100V	—
2N1363	5A	50V, 5A	75V, .5A	75V,.1A	100V	—
2N1364	5A	60V, 5A	100V, .5A	100V,.1A	120V	—
2N1365	5A	60V, 5A	100V, .5A	100V,.1A	120V	—
2N1529	10A	10V, 10A	30V, .5A	30V,.25A	40V	—
2N1530	10A	10V, 10A	45V, .5A	45V,.25A	60V	—
2N1531	10A	10V, 10A	60V, .5A	60V,.25A	80V	—
2N1532	10A	10V, 10A	75V, .5A	75V,.25A	100V	—
2N1533	10A	10V, 10A	90V, .5A	90V,.25A	120V	—
2N1534	10A	10V, 10A	30V, .5A	30V,.25A	40V	—
2N1535	10A	10V, 10A	45V, .5A	45V,.25A	60V	—
2N1536	10A	10V, 10A	60V, .5A	60V,.25A	80V	—
2N1537	10A	10V, 10A	75V, .5A	75V,.25A	100V	—
2N1538	10A	10V, 10A	90V, .5A	90V,.25A	120V	—
2N1539	10A	10V, 10A	30V, .5A	30V,.25A	40V	—
2N1540	10A	10V, 10A	45V, .5A	45V,.25A	60V	—
2N1541	10A	10V, 10A	60V, .5A	60V,.25A	80V	—
2N1542	10A	10V, 10A	75V, .5A	75V,.25A	100V	—
2N1543	10A	10V, 10A	90V, .5A	90V,.25A	120V	—
2N1544	10A	10V, 10A	30V, .5A	30V,.25A	40V	—
2N1545	10A	10V, 10A	45V, .5A	45V,.25A	60V	—
2N1546	10A	10V, 10A	60V, .5A	60V,.25A	80V	—
2N1547	10A	10V, 10A	75V, .5A	75V,.25A	100V	—
2N1548	10A	10V, 10A	90V, .5A	90V,.25A	120V	—
2N1549	20A	5V, 20A	30V, .3A	30V,.15A	40V	—
2N1550	20A	5V, 20A	45V, .3A	45V,.15A	60V	—
2N1551	20A	5V, 20A	60V, .3A	60V,.15A	80V	45V,5A
2N1552	20A	5V, 20A	75V, .3A	75V,.15A	100V	50V,5A
2N1553	20A	5V, 20A	30V, .3A	30V,.15A	40V	—
2N1554	20A	5V, 20A	45V, .3A	45V,.15A	60V	—
2N1555	20A	5V, 20A	60V, .3A	60V,.15A	80V	—
2N1556	20A	5V, 20A	75V, .3A	75V,.15A	100V	—
2N1557	20A	5V, 20A	30V, .3A	30V,.15A	40V	—
2N1558	20A	5V, 20A	45V, .3A	45V,.15A	60V	—
2N1559	20A	5V, 20A	60V, .3A	60V,.15A	80V	—
2N1560	20A	5V, 20A	75V, .3A	75V,.15A	100V	—

*A point connected by straight line between "C" and "D" for 2N629-630 and 2N1551-1552 devices only. For all other devices C-D is a straight line.

APPENDIX TO CHAPTER 2

At least four voltage-current instability considerations, where current will avalanche independently of voltage, are encountered with power transistors. These are:

1. BV_{CBO} — Breakdown Voltage Collector-to-Base, Emitter Open
2. BV_{CER} — Breakdown Voltage Collector-to-Emitter, Base Open, Where R can be 0 to ∞
3. V_{PT} — Punch-Through Voltage
4. Second Breakdown of Collector

1. — Collector-to-Base *(Emitter Open)*

BV_{CBO} is essentially the collector-base diode breakdown and for PNP germanium alloyed-junction transistors follows the relation (Reference 1):

$$BV_{CBO} = 83.4(\rho_b)^{.61} \tag{2-27}$$

where ρ_b is the resistivity of the base region.

Actually the BV_{CBO} is not always encountered in power transistors since leakage current and a surface breakdown may occur first on a nonpredictable basis. Neither type of diode breakdown is destructive if the current is limited. Excessive current will cause excessive power dissipation which can melt the junction. A typical diode breakdown voltage-current relation is shown in Figure 2-30.

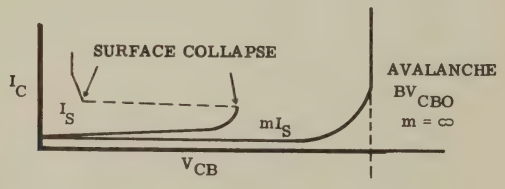


Figure 2-30 — Typical I_C Versus V_{CB}

The slight rounding of the curve of Figure 2-30 is due to the multiplication effect (m) which is related to avalanche voltage and collector voltage as follows (Reference 2):

$$m = \frac{1}{1 - \dfrac{(V_{CB})^3}{(BV_{CBO})^3}} . \tag{2-28}$$

2a. — Collector-to-Emitter; Special Case *(Base Open, $R = \infty$)*

The collector current path as a function of voltage (BV_{CEO}) with the base open is well known (Reference 3) and is affected by BV_{CBO}, current gain (h_{FB}), I_{CBO} and multiplication effect (m) in the following manner:

$$I_C = \frac{mI_{CBO}}{1 - mh_{FB}} . \tag{2-29}$$

Combining Equations 2-28 and 2-29 and dropping out an insignificant leakage effect, the collector current will be:

$$I_C = \frac{I_{CBO}}{\frac{1}{1+h_{FE}} - \frac{(V_{CE})^3}{(BV_{CBO})^3}}, \qquad (2\text{-}30)$$

where h_{FE} is low voltage common-emitter DC current gain at the I_C in question and is equal to $\frac{h_{FB}}{1-h_{FB}}$.

Since I_C approaches infinity, i.e. avalanche, when the denominator of Equation 2-30 approaches 0, the following expression is true:

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[3]{h_{FE}+1}} = \frac{83.4(\rho_b)^{.61}}{\sqrt[3]{h_{FE}+1}}. \qquad (2\text{-}31)$$

The significant point in Equation 2-31 is that BV_{CEO} is independent of I_{CBO} even though the current-voltage path to breakdown is dependent on I_{CBO} as expressed in Equations 2-29 and 2-30. Also since h_{FE} decreases as current increases, BV_{CEO} has a slight positive slope as shown in Figure 2-31. Certain transistors will have a slight negative slope in the BV_{CEO} curve at very low currents.

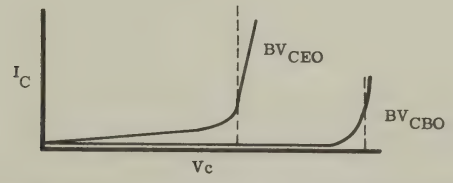


Figure 2-31 — Comparison of Typical BV_{CEO} and BV_{CBO}

2b. — Collector-to-Emitter; Special Case *(Base Shorted to Emitter, R = 0)*

The third form of breakdown, shown in Figure 2-32, occurs when the base is tied to the emitter. This is often called BV_{CES} and is the most commonly used maximum voltage rating. Generally the abrupt change in the BV_{CES} will have a negative slope, as will be explained in the following section.

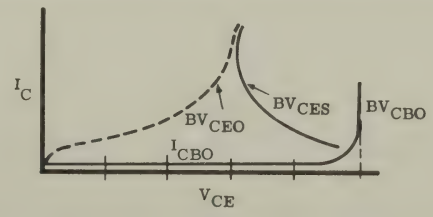


Figure 2-32 — Comparison of Typical BV_{CEO}, BV_{CES}, and BV_{CBO}

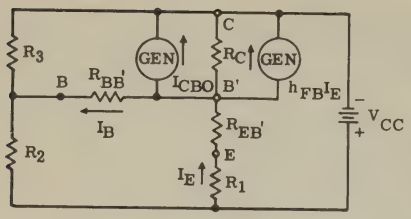


Figure 2-33
Equivalent Transistor and Bias Network

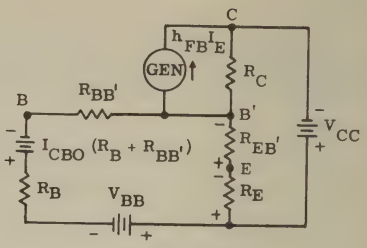


Figure 2-34
Simplified Equivalent Circuit

2c. — Collector-to-Emitter; General Case

A general equation may be derived for the I_C vs V_{CE} curve for all conditions from Base Open, Emitter Open, and Base-Emitter Shorted.

The equivalent circuit shown in Figure 2-33 and simplified in Figure 2-34 is characteristic of a PNP transistor and its external bias resistors. The collector current for the equivalent circuit is a function of collector voltage and various circuit parameters as follows:

$$I_C = \frac{mh_{FB}\, V_{BB} + h_{FB}\, mI_{CBO}\,(R_{BB'} + R_B)}{R_E + R_{EB'} + (R_{BB'} + R_B)\,(1 - mh_{FB})} \tag{2-32}$$

$$\text{where } R_B = \frac{R_2 R_3}{R_2 + R_3},$$

$$V_{BB} = \frac{R_2 V_{cc}}{R_2 + R_3}, \text{ and}$$

h_{FFB} is the low voltage common-base current gain.

By combining Equation 2-28 and 2-32 and equating the denominator to 0 so that I_C approaches infinity, an expression may be derived for the general collector breakdown voltage:

$$BV_C = BV_{CBO} \sqrt[3]{1 - \frac{h_{FB}}{1 + \dfrac{R_E + R_{EB'}}{R_B + R_{BB'}}}} \tag{2-33}$$

If the external emitter resistor (R_E) is allowed to approach infinity, BV_C will approach BV_{CBO}, which is the emitter open situation (see Equation 2-27). If R_B is very large, $BV_C = BV_{CBO} \sqrt[3]{1 - h_{FB}}$. This is the special case with the base open. If both R_E and R_B are zero, the BV_{CES} case, then the breakdown is the same as the special case of the base shorted to the emitter:

$$BV_C = BV_{CBO} \sqrt[3]{1 - \frac{h_{FB}}{1 + \dfrac{R_{EB'}}{R_{BB'}}}}. \tag{2-34}$$

It is known that under the BV_{CES} condition the voltage usually approaches BV_{CBO} (following the I_{CBO} path), then reverses and approaches BV_{CEO} as current increases The exact mechanism causing the negative resistance effect is rather complex since h_{FB}, $R_{EB'}$ and $R_{BB'}$ are functions of collector current.

Actually certain transistors do not show this effect. However, at very low I_C the emitter diode resistance, $R_{EB'}$, may be much larger than $R_{BB'}$; then $BV_{CES} \approx BV_{CBO}$. As I_C increases, $R_{EB'}$ may become smaller than $R_{BB'}$ and at a large value of I_C, $BV_{CES} \approx BV_{CEO}$. The general solution presented here is also valid where R_E and R_B are not zero and the resistance ratios can be fixed as desired such that V_C vs I_C curves will follow all possible paths between BV_{CES} and BV_{CEO}. It is also possible to use the voltage value across the junction rather than resistances to obtain the same effects. Also in the general case, I_{CBO} does not affect the breakdown voltage but does affect the path; for example, as temperature increases the BV_{CES} path approaches the BV_{CBO} path.

3. — Punch-Through *(Emitter Open)*

Another type of collector voltage effect which is independent of the others discussed is related to the collector space charge. As voltage increases the collector space charge widens until it touches the emitter space charge region thereby permitting the emitter voltage to follow the collector voltage. Transistor action ceases when the collector and emitter space charges make contact but no avalanching occurs. This effect has been labeled "Punch-Through."

The BV_{CEO} and BV_{CES} curves will be abnormal (see Figure 2-36) if the punch-through voltage occurs near their value. Common cases of punch-through are shown in Figure 2-35 and the abnormal BV_{CEO} and BV_{CES} curves are shown in Figure 2-36. Punch-through follows the equation (Reference 1):

$$V_{PT} = \frac{630W^2}{\rho_b}, \tag{2-35}$$

where W is base width in mils and ρ_b is base resistivity in ohm-cm.

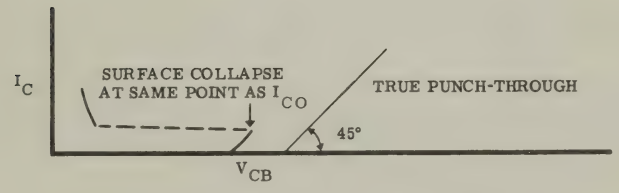


Figure 2-35 — Typical Punch-Through Action

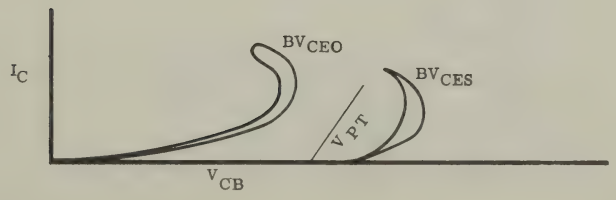


Figure 2-36 — Abnormal BV_{CEO} and BV_{CES} Curves Resulting from Low Punch-Through Voltage

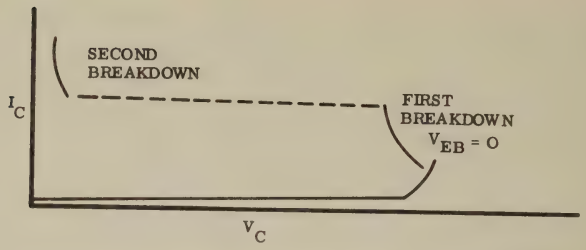


Figure 2-37 — Typical Second Breakdown Voltage Curve

4. — Second Breakdown

In the case where the V_C-I_C curve approaches BV_{CEO}, a second breakdown condition can occur if the collector current is allowed to increase without limit. This more serious voltage-current instability is generally tested with the base tied to the emitter. When it occurs, the voltage drops suddenly to a low value as shown in Figure 2-37.

When second breakdown was first observed, during BV_{CES} testing of 2N176 transistors it was thought to occur only when $V_{EB} = 0$ or when the base was positive with respect to the emitter. These tests often caused irreversible changes in the voltage-current relationship and some units actually shorted between emitter and collector so that the junctions acted as diodes tied together. Upon dissection the shorted devices showed a small hole through the base wafer, usually near its geometrical center.

This physical action of second breakdown is thought to be due to a "Pinch" effect which develops when a large positive base bias causes the current flow to channel into an ever-shrinking area. The power dissipation is concentrated in a very small area and the resultant temperature rise melts the junctions together.

Further investigations have shown that second breakdown can occur with the base physically and electrically open (BV_{CEO} case). Also it was discovered that both positive and negative base drive will set the trigger and a complete locus of these trigger points is shown in Figure 2-38.

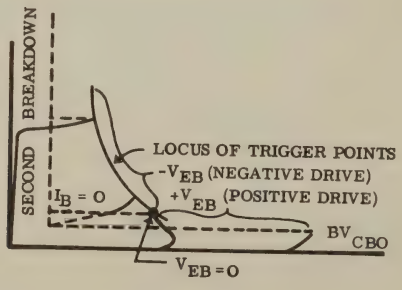


Figure 2-38 — Locus of Second Breakdown Trigger Points

The second breakdown voltage is always the same regardless of where triggered, although negative drives do not seem to cause irreversible changes as easily as positive ones. The pin hole occurs near the center of the junction for negative as well as positive drive, which seems to disprove the "Pinch" effect theory since the emitter current should then be spread to the outer edge of the junction.

Second breakdown also occurs with the emitter open if diode avalanche current is allowed to increase to high values. This indicates that the phenomenon occurs in the collector junction but can be controlled in the emitter junction. It must be kept in mind that the above discussion is based on typical behavior of power transistors. Actual voltage-current plots of a large group of transistors will show many extreme variations.

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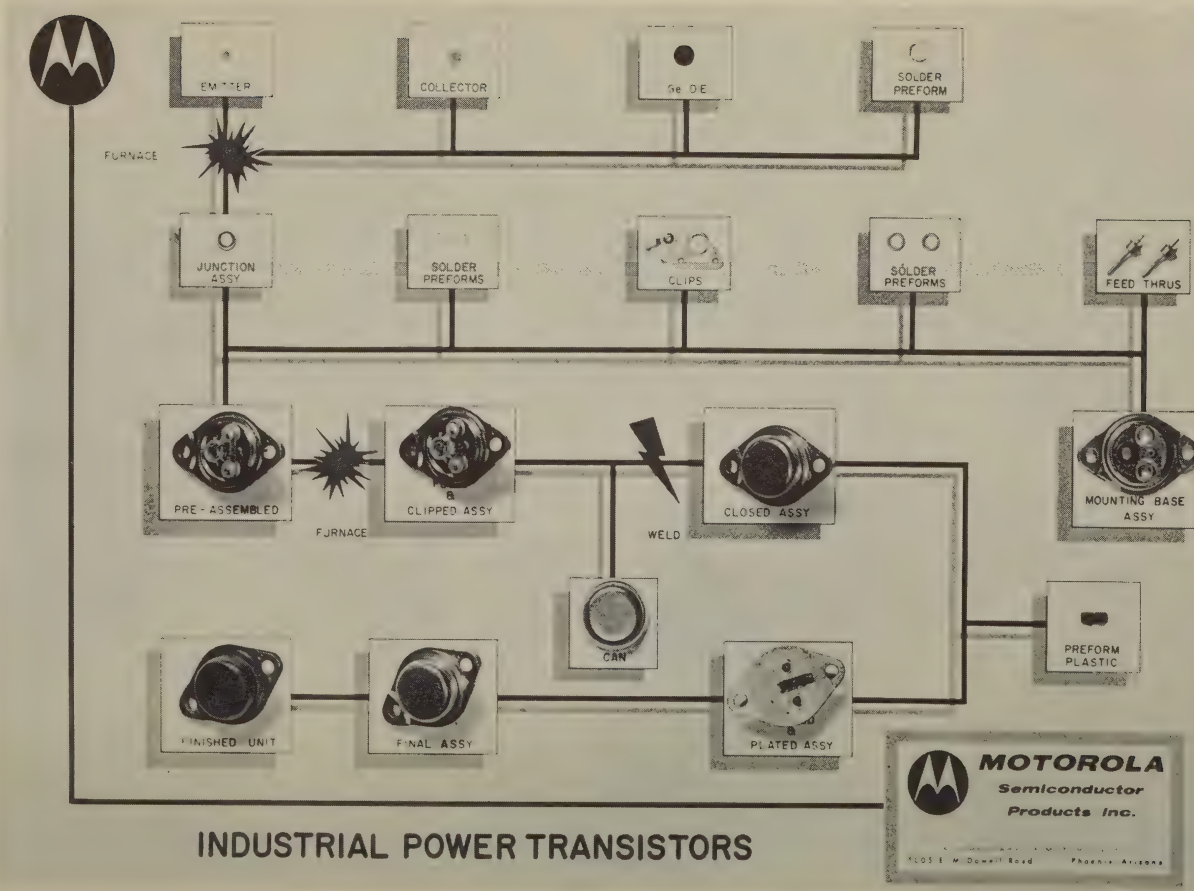
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CHAPTER III

Power Amplifiers

3-1 — Bias Considerations

Bias voltage on the emitter junction determines collector current just as grid bias determines plate current in a vacuum tube. The definitions of Class A, B, and C operation which apply to tubes also apply to transistors. Class A allows 360-degree operation of a sine wave. Class B is with zero bias (cutoff) and allows 180-degree conduction. Class C is biased beyond cutoff and allows less than 180-degree conduction. Another commonly used bias is Class AB which allows small-signal Class A operation and large-signal Class B operation. These classes of operation are illustrated in Figure 3-1.

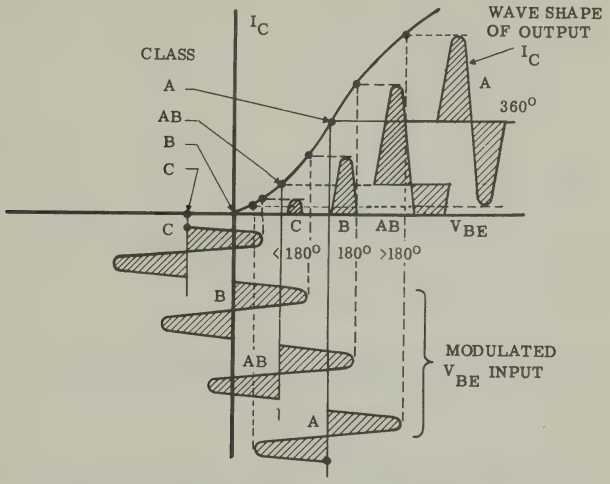


Figure 3-1 — Waveshapes of Classes of Operation

The collector voltage is determined by the collector supply voltage, the D-C load resistance, and the collector current. The simple circuit of Figure 3-2 illustrates a complete bias arrangement. Input and output bias are interrelated through the current gain or transconductance transfer function. The transistor operation can be represented graphically by a combination of input, transfer, and output curves. In addition, all D-C and A-C external resistors are graphically represented in Figure 3-3.

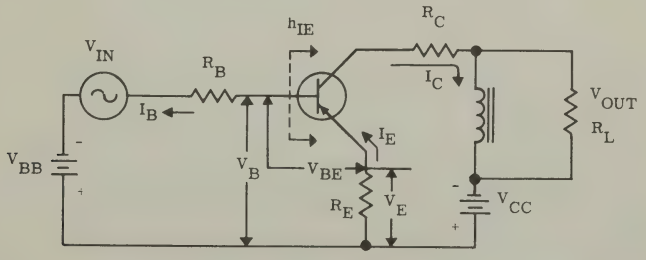


Figure 3-2 — Typical Class A Amplifier with Bias

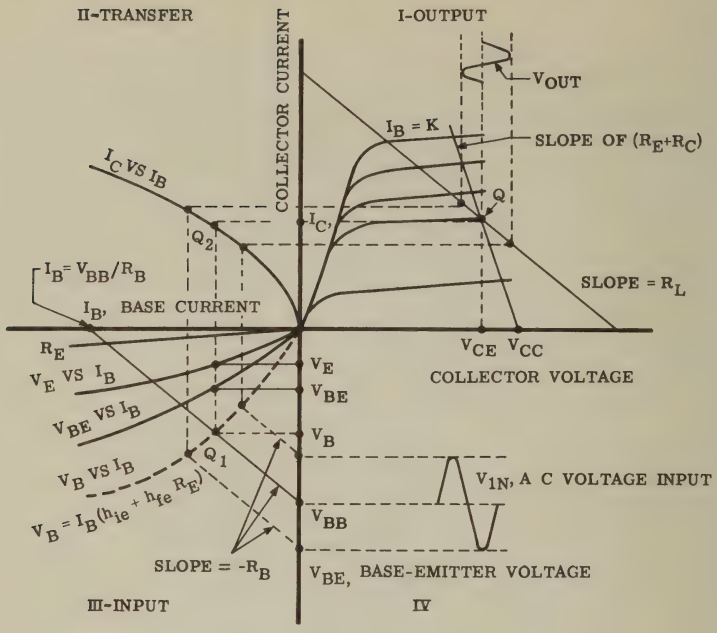


Figure 3-3 — Graphical Analysis of Typical Class A Operating Conditions Using Current Gain Curve

Figure 3-3 completely describes the operation of a typical Class A audio amplifier. Both D-C and A-C conditions are obtainable from this composite curve. The D-C conditions will be described first.

The area in the third quadrant concerns the emitter-base junction or the input. The vertical axis represents the voltage and the horizontal the current. If the transistor is removed and no base current flows, the input voltage, V_B, will equal V_{BB}. If the transistor and R_E were replaced with a direct short, V_B would be zero and the base supply current would equal $\frac{V_{BB}}{R_B}$. When the transistor and R_E are inserted, the input operating point, Q_1, will be established where the $-R_B$ slope intersects the composite $(h_{IE} + h_{FE} R_E)$ curve, where h_{IE} is the input resistance of the transistor. This composite curve relates base current to voltage drop from base to common emitter. If R_E were zero, the Q_1 point would be at the intersection of $-R_B$ and the V_{BE} vs I_B curve.

The effect of R_E on the input (in this case the base) is amplified by the current gain of the transistor. The equivalent resistance network is shown in Figure 3-4. The input network is composed of two resistances h_{IE} and the equivalent h_{FE} x R_E. The source network is composed of a D-C voltage source, V_{BB}, an A-C voltage source, V_{IN}, and a source resistance R_B. The base current can be thought of as circulating through the entire network.

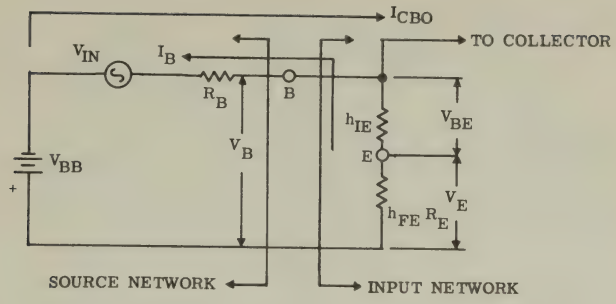


Figure 3-4 — Equivalent Input Circuit

The relationships of base current and the voltage drops in the input circuit may be graphically constructed to form the input quadrant of Figure 3-3. The I_B vs V_{BE} line relates the base current and the voltage across h_{IE}. The I_B vs V_E line shows the effect of voltage drop across the equivalent resistor $h_{FE}R_E$. This is a curved line since current gain decreases as current increases. The two curves may be added in the voltage direction to obtain the series total curve I_B vs V_B.

The input point, Q_1, determines a certain base current, I_B, which, projected onto the I_C vs I_B transfer curve (Quadrant II), establishes another operating point, Q_2. This transfer point then determines the magnitude of the collector current, I_C.

The collector current in the output Quadrant I is essentially independent of collector voltage, while the collector-emitter voltage is determined in the following manner. Consider the transistor removed from the circuit so there is zero collector current. The voltage at the collector terminal then equals V_{CC}. If the transistor is replaced with a wire of negligible resistance (with R_E in place), the collector supply current equals $\frac{V_{CC}}{(R_E + R_C)}$. (This point, not shown on the graph, is on the vertical axis where $V_{CE} = 0$.) The line joining these two points, V_{CC} and $\frac{V_{CC}}{R_E + R_C}$, establishes the negative slope of $(R_E + R_C)$. The output operating point, Q, is where the slope of $(R_E + R_C)$ intersects the collector current projected from the transfer point Q_2.

The A-C conditions are projected in the same manner as the D-C. The projection of the sine wave in Quadrant IV illustrates the manner in which a small signal inserted into the base is amplified and transferred to the load. Note, however, that in Quadrant I the time-variable part of the signal is projected onto the line labeled "slope of $-R_L$" (the A-C load line) rather than the slope of the $-(R_C + R_E)$ line — at zero signal level these two lines intersect. The A-C R_B is usually not the same as the D-C R_B.

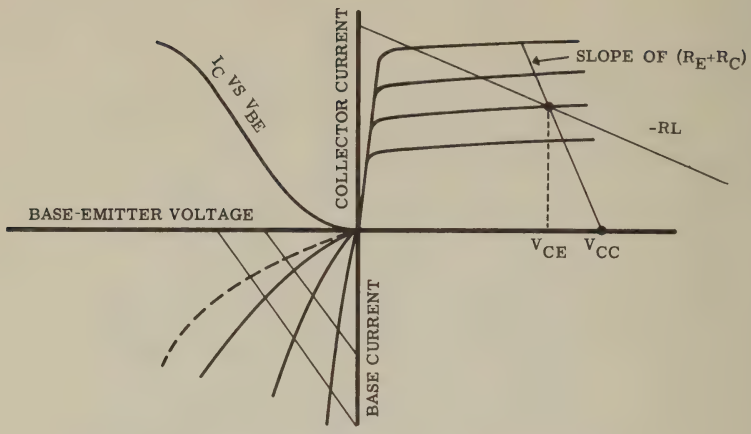


Figure 3-5 — Graphical Analysis Using Transconductance Curve

If the transconductance transfer curves are available, the combination curves in Figure 3-5 will be useful. The description of this set of curves is the same as that discussed for Figure 3-3.

While the circuit shown in Figure 3-2 was for illustrative purposes, it also represents the simplest equivalent circuit for one- or two-battery systems. Generally only one battery is used, as shown in Figure 3-6.

The graphical method of determining collector current has been discussed but basic circuit equations give much information that graphs cannot give. For instance, while the effect of I_{CBO} upon bias is very important, it is difficult to derive exact information graphically. However, it is possible to draw the D-C equivalent of Figure 3-6, as shown in Figure 3-7, and write the equation for the external circuit as well as the equation for emitter current in terms of transistor and circuit parameters.

$$R_B = \frac{R_1 R_2}{R_1 + R_2}, \tag{3-1}$$

$$R'_B = R_B + R_3, \tag{3-2}$$

$$V_{BB} = \frac{R_B}{R_2} \times V_{CC}. \tag{3-3}$$

Since R_C has little effect on emitter current, only the emitter and base conditions are considered here. The circuit of Figure 3-7 can be represented in the form of Figure 3-8A which includes the equivalent circuit of the transistor itself. This circuit can be further simplified by transferring $R'_B + R_{BB}'$ into the emitter lead and inserting a battery (of the same polarity as V_{BB}) in the base lead equal to $I_{CBO}(R'_B + R_{BB}')$. This simplified circuit is shown in Figure 3-8B.

Solving for emitter current in the circuit of Figure 3-8,

$$I_E = \frac{V_{BB} - V_{B'E} + I_{CBO}(R'_B + R_{BB}')}{R_E + \dfrac{R'_B + R_{BB}')}{h_{FE} + 1}} \tag{3-4}$$

where $V_{B'E}$ is the emitter diode voltage at a specific I_E.

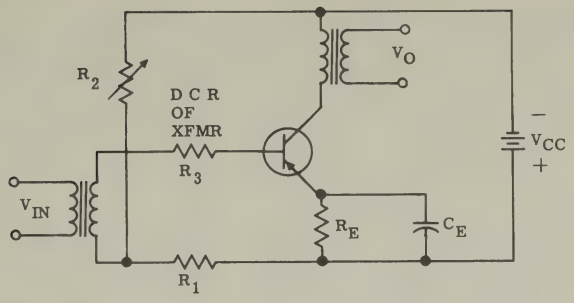


Figure 3-6 — Basic Single-Ended One-Battery Power Amplifier

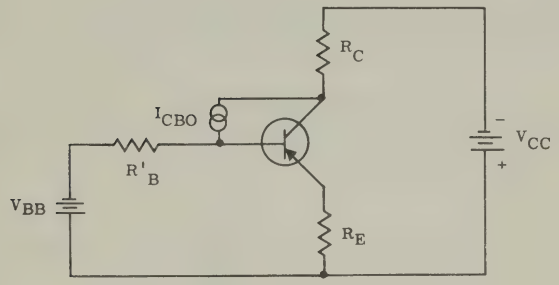


Figure 3-7 — Equivalent DC Circuit of Figure 3-6

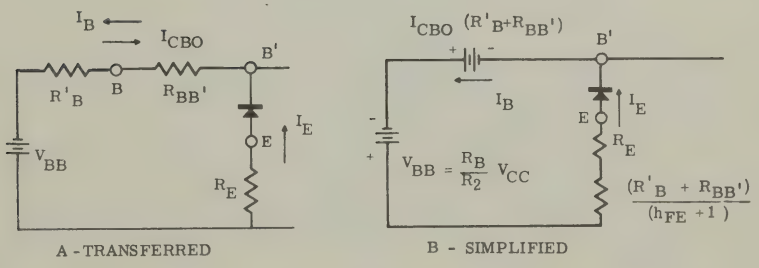


Figure 3-8

A — Transferred Equivalent Circuit

B — Simplified Equivalent Circuit

3-2 — Stability

It is important to maintain a fixed operating point, unchanged by transistor and temperature variations. If the Q point were to drift, a large portion of the output wave shape would be clipped on one or the other peaks. This may be seen by shifting the Q point on the graphs of Figure 3-3 or 3-5. Also, as will be explained later in the section, too much shift can cause thermal runaway. Thus stability is always a prime consideration.

The factors that are affected by temperature are $V_{B'E}$, I_{CBO}, and h_{FE}. As in any germanium diode, $V_{B'E}$ has a negative temperature coefficient of approximately 1.8 mw/°C. The current gain, h_{FE}, can have either a positive or negative temperature coefficient, depending on the value of emitter current. Usually, at low emitter currents, the coefficient is positive. As emitter current increases, a point will be reached at which the coefficient is zero. Above this point, coefficients are negative. At low voltages I_{CBO} will double approximately every 10°C. A curve for I_{CBO} versus temperature is shown in Figure 3-12.

Examination of Equation 3-4 indicates that to minimize the effects of h_{FE} on the operating point, Q, R'_B should be small and R_E large. This is shown graphically in Figure 3-9, which is based upon the combined characteristic curves of Figure 3-3.

Figure 3-9 shows that the change of collector current, I_C, as a function of gain is reduced by increasing the emitter resistor, R_E. With an emitter resistance present, an increase of base resistance, R'_B, will increase the change in I_C with an increase in gain.

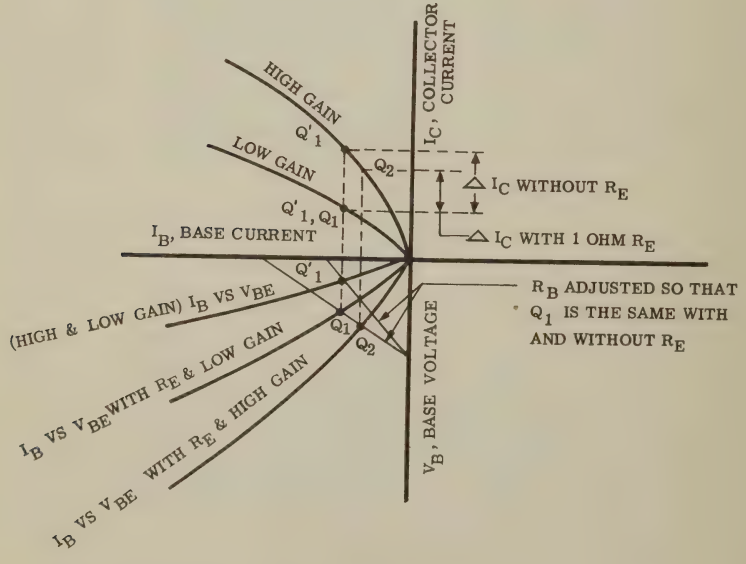


Figure 3-9 — Effect of R_E Upon Stability

I_{CBO}, as well as current gain, affects I_E. Equation 3-4 shows that to reduce the effect of I_{CBO} (assuming h_{FE} to be constant), R'_B should be small. The I_{CBO} influence on I_C or I_E is best represented by what is called stability factor, which relates the change of I_E as a change of I_{CBO} due to an increase in temperature.

The current stability factor is defined as

$$S_I = \frac{\Delta I_E}{\Delta I_{CBO}}, \tag{3-5}$$

and by differentiating Equation 3-4,

$$S_I \approx \frac{R'_B + R_{BB'}}{R_E + \dfrac{R'_B + R_{BB'}}{h_{FE} + 1}} = \frac{1}{\dfrac{R_E}{R'_B + R_{BB'}} + \dfrac{1}{h_{FE} + 1}}. \tag{3-6}$$

Several important considerations are indicated by the stability equations. For instance as R_E increases, the current stability factor decreases (also shown by the graphical analysis of Figure 3-9). As R_B' decreases, the stability also decreases due to less resistance in the base circuit from which I_{CBO} can develop a bias voltage. As gain, h_{FE}, increases, the S_I increases. At very high current gain

$$S_I = \frac{R'_B + R_{BB'}}{R_E}. \tag{3-7}$$

The voltage stability factor is defined as

$$S_V = \frac{\Delta V_{CE}}{\Delta I_{CBO}}, \tag{3-8}$$

and for the circuit of Figure 3-7 is

$$S_V \approx -S_I(R_E + R_C) - R_C. \tag{3-9}$$

Power transistors usually are transformer coupled and the resistance R_C in series with the collector is virtually zero. Hence,

$$S_V = -S_I R_E. \tag{3-10}$$

The current stability factor is difficult to keep below 10 without excessive power losses in most power transistor circuits. Since high temperature I_{CBO} can be on the order of 10 mA, the ΔI_E can be as much as 100 mA. The stability equation will generally provide an approximation of emitter current shift as a function of temperature, but because gain and base-emitter voltage also vary with temperature, the following equations will provide a more exact method of determining values of the bias network resistors.

3-3 — Resistive Bias Design Equations

From data sheets and supplementary information the following must be known:

$h_{FE\ min}$, $h_{FE\ max}$, $V_{BE\ min}$, $V_{BE\ max}$,
$I_{CBO\ min}$, $I_{CBO\ max}$, $I_{E\ max}$, and R_E.

Generally, the voltage across R_E is set to a fixed value — about 0.5V to 1.0V — in order to reduce the effect of changes in the emitter diode voltage. These values take into account all variations due to transistor characteristic spreads and temperature change from $T_{J\ min}$ to $T_{J\ max}$. Motorola industrial power transistors have a $T_{J\ max}$ of 100°C. The minimum T_J is determined with the following equation:

$$\theta_{JA} = \frac{T_{J\ max} - T_{A\ max}}{V_{CE} I_{E\ max}} = \frac{100 - T_{A\ max}}{V_{CE}\ I_{max}}. \tag{3-11}$$

Substituting minimums for the maximum values in the above equation:

$$T_{J\ min} = V_{CE} I_{E\ min} \theta_{JA} + T_{A\ min}. \tag{3-12}$$

$I_{E\ max}$ and $I_{E\ min}$ can be written in terms of the known information with a modification of Equation 3-4 to include $R_{BB'}$ as part of V_{BE}. Emitter current is a maximum when V_{BE} is a minimum and I_{CBO} and h_{FE} are maximum.

$$I_{E\ max} = \frac{\frac{R_B V_{CC}}{R_2} - V_{BE\ min} + I_{CBO\ max} R'_B}{R_E + \frac{R'_B}{(h_{FE\ max} + 1)}}. \tag{3-13}$$

$$I_{E\ min} = \frac{\frac{R_B V_{CC}}{R_2} - V_{BE\ max} + I_{CBO\ min} R'_B}{R_E + \frac{R'_B}{(h_{FE\ min} + 1)}}. \tag{3-14}$$

Solving equations 3-13 and 3-14 for R_2:

$$R_2 = \frac{R_B V_{CC}}{I_{E\ max}\left[R_E + \frac{R'_B}{(h_{FE\ max} + 1)}\right] + V_{BE\ min} - I_{CBO\ max} R'_B}. \tag{3-15}$$

$$R_2 = \frac{R_B V_{CC}}{I_{E\ min}\left[R_E + \frac{R'_B}{(h_{FE\ min} + 1)}\right] + V_{BE\ max} - I_{CBO\ min} R'_B}. \tag{3-16}$$

Solving Equations 3-15 and 3-16 simultaneously for the value of the equivalent base resistance R'_B:

$$R'_B = \frac{(I_{E\,max} - I_{E\,min})\, R_E + V_{BE\ min} - V_{BE\ max}}{\frac{I_{E\ min}}{h_{FE\ min} + 1} - \frac{I_{E\ max}}{h_{FE\ max} + 1} + I_{CBO\ max} - I_{CBO\ min}}. \tag{3-17}$$

If $R_{BB'}$ is considered separately, the V_{BE} terms must be replaced by $V_{B'E}$ and the value of $R_{BB'}$ must be subtracted from the entire term on the right hand side of Equation 3-17.

From Equation 3-2

$$R_B = R'_B - R_3. \tag{3-18}$$

Usually R_3 is known and from Equation 3-1

$$R_1 = \frac{R_B R_2}{R_2 - R_B} . \tag{3-19}$$

The following is an example showing how to use these equations to determine the bias network resistor values.

Given:

$V_{CE} = 12$ volts

$I_{E\ min} = 500$ mA

$I_{E\ max} = 600$ mA

$T_{A\ min} = 25°C$

$T_{A\ max} = 40°C$

$T_{J\ max} = 100°C$

$R_E = 2\Omega$ (based upon dropping 1 volt across R_E as previously discussed)

$R_3 = 1.4\Omega$ (assumed value of D-C resistance of driver transformer secondary)

To find $T_{J\ min}$, assume worst conditions (maximum power at maximum temperature). θ_{JA}, thermal resistance from junction to ambient, is, from Equation 3-11,

$$\theta_{JA} = \frac{T_{J\ max} - T_{A\ max}}{V_{CE} \times I_{E\ max}} = \frac{100 - 40}{12 \times 0.6} = 8.3°C/W.$$

From Equation 3-12

$$T_{J\ min} = V_{CE} \times I_{E\ min} \times \theta_{JA} + T_{A\ min} = 12 \times 0.5 \times 8.3 + 25 = 75°C.$$

Assume that for 75°C, the minimum I_{CBO} is 1 mA, and the maximum value at 100°C is 20 mA. Generally the minimum I_{CBO} is almost negligible; the maximum value is found in the data sheet.

The range of V_{BE} and h_{FE} at the extreme junction temperatures can be found in Figures 3-10 and 3-11. Similar curves are generally found in the data sheet.

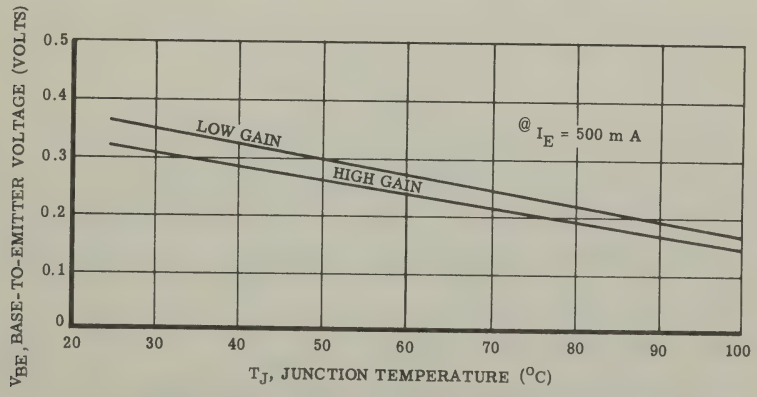


Figure 3-10 — Typical Power Transistor V_{BE} Versus T_J

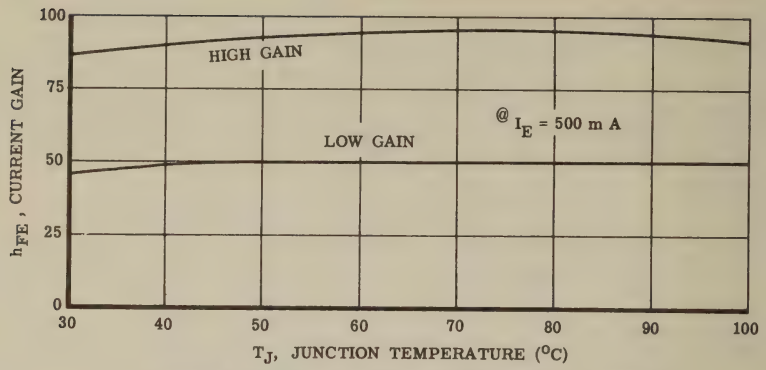


Figure 3-11 — Typical Power Transistor h_{FE} Versus T_J

$V_{BE\ max} = 0.23$ volt (at 75°C)
$V_{BE\ min} = 0.15$ volt (at 100°C)
$h_{FE\ max} = 90$ (at 75°C)
$h_{FE\ min} = 50$ (at 100°C)

Find the bias network values, R'_B, R_B, R_2, and R_1.
From Equation 3-17:

$$R'_B = \frac{(0.6 - 0.5)2 + 0.15 - 0.23}{\frac{0.5}{51} - \frac{0.6}{91} + 0.02 - 0.001} = \frac{0.12}{0.0223} = 5.4\Omega$$

From Equation 3-18:

$$R_B = 5.4 - 1.4 = 4\Omega$$

From Equations 3-15 or 3-16:

$$R_2 = \frac{4 \times 12}{0.5\left(2 + \frac{5.4}{50 + 1}\right) + 0.23 - 0.001 \times 5.4} = 37.8\Omega$$

From Equation 3-19:

$$R_1 = \frac{4 \times 37.8}{37.8 - 4} = 4.5$$

Note: It is possible to arrive at negative values or extremely low positive values of R'_B. Such cases can be handled by increasing the value of R_E or allowing a greater range of I_E to provide practical values of R'_B.

For Class AB operation, the network is solved for one transistor. The values found are twice the actual value of R_1 and R_2.

Quite often the above design results in excessively large values of R_E. Thermistor control is then required.

3-4 — Designing with a Thermistor

Thermistors are negative temperature coefficient resistors used in place of or in parallel with *either* R_1 or R_2 (Figure 3-6) to compensate for variations

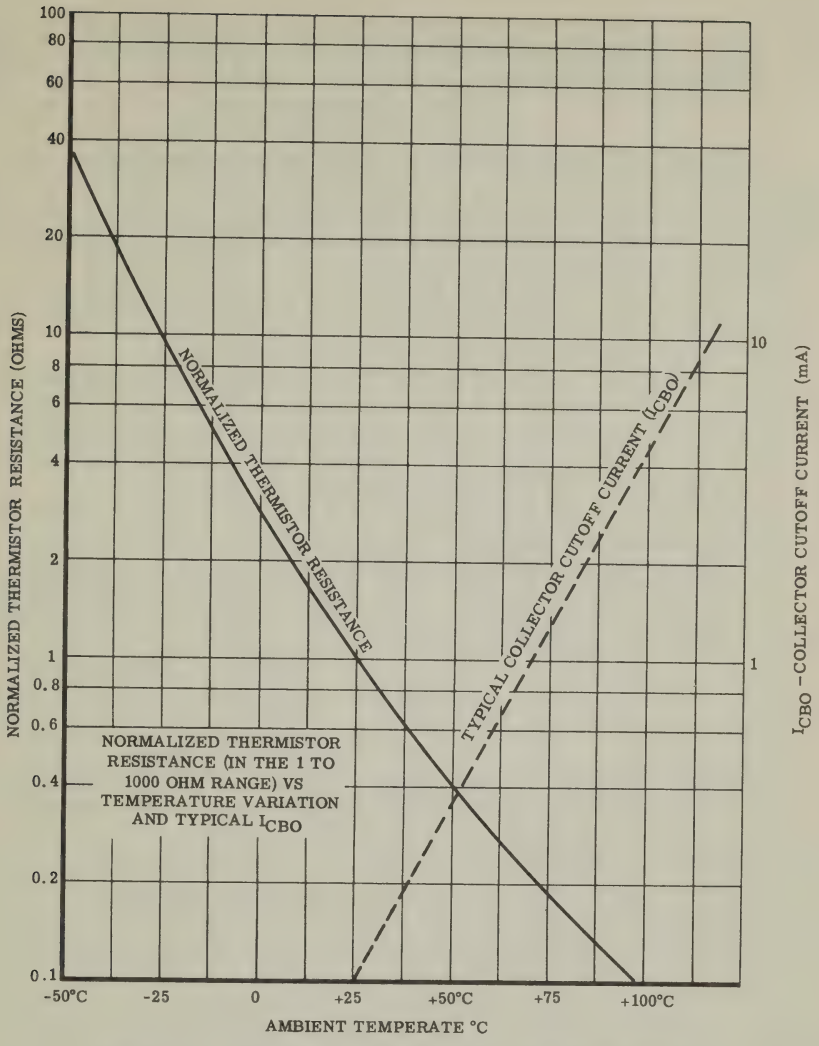


Figure 3-12 — Thermistor Value and I_{CBO} Versus Temperature

in emitter current because of temperature change. The parallel combination of R_1 and R_2, namely R_B of Equation 3-1, is actually the factor for which compensation is required.

It is possible that one thermistor or two thermistors with or without fixed shunt resistors may be necessary.

A thermistor cannot be used in place of R_2 or in parallel with R_2 because self-heating will cause its resistance value to continue to decrease. This is because a nearly constant voltage is imposed upon it.

A normalized thermistor curve is shown in Figure 3-12 along with a typical I_{CBO} power transistor curve. To find the value of any thermistor in the range 1 to

1000 ohms and 50°C to +100°C, the value at 25°C is multiplied by the normalized factor as found from the curve. For instance at 50°C a thermistor having a value of 25 ohms at 25°C would be

$$0.4 \times 25 = 10 \text{ ohms at } 50°\text{C}.$$

Graphical curve-shaping techniques have been developed which make it possible to design compensating networks covering a wide temperature range. Reference 5 provides a good treatment of this method. The equivalent R'_B is found as a function of temperature either experimentally or calculated with Equation 3-17.

A two-temperature method, which is simpler and usually adequate is described below. This method does not provide tracking but will keep I_E within limits at the two temperature extremes.

1. Equation 3-17 will be solved for R'_B at minimum ambient temperature, $T_{A\ min}$, and another value of R'_B at maximum ambient temperature, $T_{A\ max}$. All resistors and voltages associated with $T_{A\ min}$ will use the subscript C for cold, and with $T_{A\ max}$, an H for hot. Thus in this step we find R'_{BC} and R'_{BH}.
2. Solve for R_{2C} and R_{2H} using Equation 3-15 or 3-16.
3. Solve for R_{BC} and R_{BH} using Equation 3-18, assuming a practical value for the transformer secondary D-C resistance R_3.
4. Solve for R_{1C} and R_{1H} with Equation 3-19.
5. The values obtained in Step 4 are the equivalent parallel-series resistance combinations of fixed resistors and thermistors. The general equation to find the thermistor value in parallel with a fixed resistor is

$$R_{TC} = \frac{R_{PC}R_{PH}(1-K)}{K(R_{PC}-R_{PH})}, \tag{3-20}$$

where

R_{PC} is the cold value of the parallel combination of a fixed resistor and a thermistor. R_{PC} may turn out to be either R_1 or both R_1 and R_2.

R_{PH} is the hot value of the parallel combination.

R_{TC} is the cold thermistor value, and

K is the ratio of the hot thermistor value to the cold value as found in Figure 3-12.

The general value of the fixed resistor is

$$R = \frac{R_{TC}R_{PC}}{R_{TC}-R_{PC}}, \tag{3-21}$$

where R is the fixed resistor and is not temperature dependent.

Note: The above equations apply only when R_{PH} is greater than KR_{PC}. When $R_{PH} = KR_{PC}$, the fixed resistors are infinite. When R_{PH} is less than KR_{PC}, the above design is impossible and either closer tolerance transistors must be used or a greater I_E range allowed.

The following is a modified version of the two-temperature method which uses a potentiometer in place of R_2. The potentiometer provides a gain adjustment to correct for characteristic distributions at room temperature of various units of the same type. Then a thermistor-resistor combination for R_1 will correct for characteristic shifts caused by an increase or decrease of temperature. The transistor with the lower gain will require the lower value of R_2. The method to find the circuit values is a "cut and try" one. The cold temperature limit set-

tings for R_2 are found in conjunction with a value of R_1. Then a thermistor is selected to control the I_E of the higher gain transistor at the hot temperature. Next the I_E of the lower gain transistor is checked to determine whether it is still within limits. Summarizing then six steps:

1. Arbitrarily choose R_E and the cold R_{BC}.
2. Solve for the cold R'_{BC} with a modified form of Equation 3-18:

$$R'_{BC} = R_{BC} + R_3 \tag{3-22}$$

3. Determine the value of R_2 for the high and low gain limits. A modified form of Equation 3-15 with all values at the cold temperature is used:

$$R_{2\,max} = \frac{R_{BC}V_{CC}}{I_E\left[R_E + \dfrac{R'_{BC}}{h_{FE\,max}+1}\right] + V_{BE\,min} - I_{CBO}R'_{BC}}$$

$$R_{2\,min} = \frac{R_{BC}V_{CC}}{I_E\left[R_E + \dfrac{R'_{BC}}{h_{FE\,min}+1}\right] + V_{BE\,max} - I_{CBO}R'_B} \tag{3-23}$$

(3-24)

The value of $R_{2\,min}$ should be at least ten times the value of R_{BC} to minimize an error resulting from the effect of R_2 on the value of R_{BC}. Note also the higher gain transistor will almost always have the lower V_{BE}.

4. The hot R_{BH} must now be computed by rearranging Equation 3-15 and solving for R_B.

$$R_{BH} = \frac{I_{E\,hot}\left[R_E + \dfrac{R_3}{h_{FE\,hot}+1}\right] + V_{BE\,hot} - I_{CBO\,hot}R_3}{\dfrac{V_{CC}}{R_{2\,max}} + I_{CBO\,hot} - \dfrac{I_{E\,hot}}{h_{FE\,hot}+1}} \tag{3-25}$$

Values selected are those associated with the higher gain transistor at the hot temperature.

5. Insert into a modified Equation 3-13 the value of R_{BH} and the other characteristic values of the lower gain transistor at the hot temperature:

$$I_{E\,hot} = \frac{\dfrac{R_{BH}V_{CC}}{R_{2\,min}} - V_{BE\,hot} + I_{CBO\,hot}(R_{BH}+R_3)}{R_E + \dfrac{R_{BH}+R_3}{h_{FE\,hot}+1}} \tag{3-26}$$

If this $I_{E\,hot}$ value is not within the allowable limits the values of R_E and R_B must be adjusted until it does.

6. The parallel network or R_1 and R_{TC} which forms R_B now is determined from modified versions of Equations 3-20 and 3-21:

$$R_{TC} = \frac{R_{BC}R_{BH}(1-K)}{K(R_{BC}-R_{BH})} \tag{3-27}$$

$$R_1 = \frac{R_{TC}R_{BC}}{R_{TC}-R_{BC}} \tag{3-28}$$

Example (using potentiometer and thermistor, see Figure 3-13):

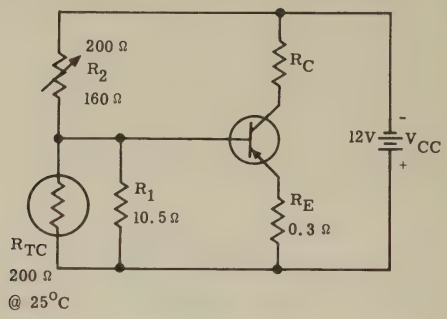


Figure 3-13 — Thermistor Control

Given:

	Cold	*Hot*
T_A	25°C	75°C
T_J	35°C	85°C
I_E	0.5A (min)	0.6A (max)
I_{CBO}	0.2 mA	4.0 mA
$h_{FE\ max}$	100 (high gain transistor)	120
$h_{FE\ min}$	50 (low gain transistor)	60
$V_{BE\ max}$	0.5 V (low gain transistor)	0.4 volt
$V_{BE\ min}$	0.4 V (high gain transistor)	0.3 volt
V_{CC}	12 V	12 V

Find:

Values of potentiometer, R_1 and R_{TC}.

Solution:

1. Let $R_E = 0.3\Omega$ and $R_{BC} = 10\Omega$.
2. From Equation 3-22 assume $R_3 = 0$. Then $R'_{BC} = 10\Omega$
3. From Equation 3-23

$$R_{2\ max} = \frac{10 \times 12}{0.5\left[0.3 + \frac{10}{100+1}\right] + 0.4 - 0.2 \times 10^{-3} \times 10}$$

$$R_{2\ max} = 200\Omega$$

From Equation 3-24

$$R_{2\ min} = \frac{10 \times 12}{0.5\left[0.3 + \frac{10}{50+1}\right] + 0.5 - 0.2 \times 10^{-3} \times 10}$$

$$R_{2\ min} = 160\Omega$$

4. From Equation 3-25, for the higher gain transistor:

$$R_{BH} = \frac{0.6\,[0.3 + 0] + 0.3}{\frac{12}{200} + 4 \times 10^{-3} - \frac{0.6}{120 + 1}}$$

$$R_{BH} = 8.14\Omega$$

5. From Equation 3-26 for lower gain transistor

$$I_{E\ hot} = \frac{\frac{8.14 \times 12}{160} - 0.4 + 4 \times 10^{-3} \times 8.14}{0.3 + \frac{8.14}{60 + 1}}$$

$I_{E\ hot} = 0.557A$, which is in limits.

6. For this example K = 0.18 at 75°C (from Figure 3-12). From Equation 3-27:

$$R_{TC} = \frac{10 \times 8.14(1 - 0.18)}{0.18(10 - 8.14)}$$

$R_{TC} = 200\Omega$ thermistor.

From Equation 3-28:

$$R_1 = \frac{200 \times 10}{200 - 10} = 10.5\Omega \text{ resistor.}$$

The complete circuit is shown in Figure 3-13.

Other temperature compensated (T.C.) resistors are available which do not change with temperature as much as thermistors. These have both negative and positive coefficients. The positive type may be used in place of R_E or R_2 of Figure 3-6.

3-5 — Diode Stabilization

The use of one or two diodes to provide stabilization is also a very efficient method of temperature compensating power transistors. Two such circuits are shown in Figures 3-14 and 3-15.

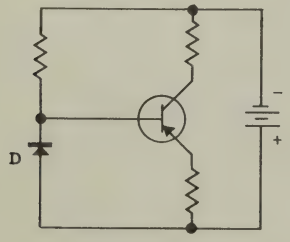


Figure 3-14 — Single Diode Compensation

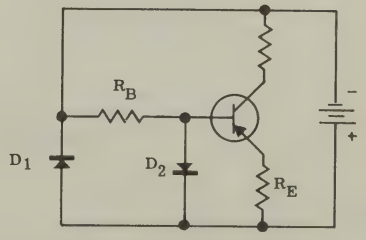


Figure 3-15 — Two Diode Compensation

The single-diode method of compensation is based on the assumption that the forward voltage drop across the diode (which has a negative temperature coefficient of 1.8 mv/°C) will compensate for the change in V_{BE}. However V_{BE} can have either positive, negative, or zero change with temperature, so the diode method is suitable only in specialized cases.

The two-diode method uses one diode, D_1, in the same manner as the single diode in the method discussed above. The second diode, D_2, is reversed biased and should have a leakage current, I_{CBO}, somewhat larger than the transistor I_{CBO}. Diode D_2 allows an I_{CBO} path which is in series with the transistor collector diode. This provides a low voltage drop for I_{CBO} without affecting normal bias settings. When D_1, D_2, R_B, and R_E are at optimum values, excellent stability will usually result. Normally these values are determined by experimental methods although graphical methods such as shown in Figures 3-3, 3-5, and 3-9 can be of assistance.

3-6 — Testing of Stability

Stability should be tested throughout the entire temperature range. All prototype circuits should be completely tested with as many possible combinations of the variables as is practical. If I_{CBO} is the only suspected cause of unstable operation, a simple room temperature check can be made using an I_{CBO} simulator. This simulator, described in Figure 3-16, injects a constant current (equal to the value of I_{CBO} at the hot temperature) into the base. The stability of the circuit is checked by monitoring emitter or collector current. Collector current is usually monitored because the meter resistance will not upset the circuit. The value of R_{CBO} should be at least ten times the value of R'_B of Equation 3-2.

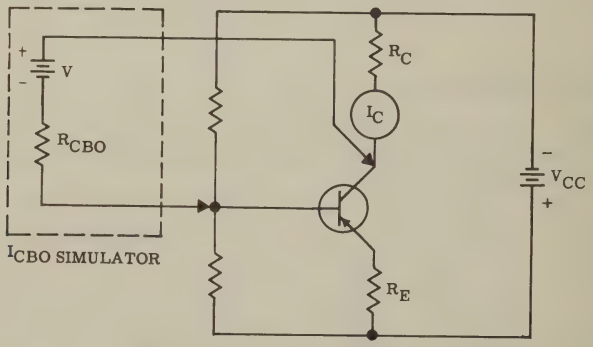


Figure 3-16 — I_{CBO} Simulator

3-7 — Thermal Runaway

Thermal runaway occurs when the junction temperature builds up because the heat sink is not capable of dissipating heat fast enough. If all other transistor characteristics are temperature independent, the I_{CBO} factor increasing with temperature causes a regeneration effect on junction temperature.

Consider that the term $S_I \times I_{CBO} \times V_{CE}$ is the D-C power loss in excess of the normal power loss $I_C V_{CE}$. This additional power dissipation causes a rise in junction temperature which increases I_{CBO}, in turn creating more power dissipation and so on. The final junction temperature can be expressed as:

$$T_J = T_A + \theta_{JA} I_E V_{CE} + \theta_{JA} S_I V_{CE} I_{CBOTJ}. \quad (3\text{-}29)$$

Also, for germanium transistors:

$$I_{CBOTJ} = I_{CBOTO} \times \epsilon^{\left[\frac{(T_J - T_O)\ 8350}{T_O T_J}\right]}, \quad (3\text{-}30)$$

where T_O is some reference temperature and I_{CBOTO} and I_{CBOTJ} are the collector cutoff currents measured at T_O and T_J respectively. The value, 8350, is a constant associated with the germanium junction.

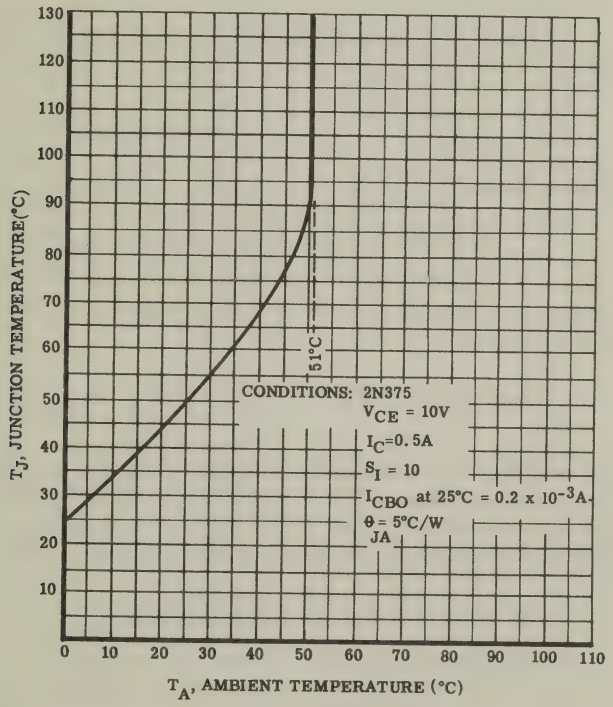


Figure 3-17 — Thermal Runaway for a Typical Condition

Therefore,

$$T_J = T_A + \theta_{JA} I_E V_{CE} + \theta_{JA} S_I V_{CE} I_{CBOTO}\, \epsilon^{\left[\frac{(T_J - T_O)\ 8350}{T_O T_J^*}\right]}. \quad (3\text{-}31)$$

*T_J and T_O in the exponential term must be expressed in degrees Kelvin. (Add 273° to all Centigrade readings.) All other temperatures are in degrees Centrigrade. A plot of T_A vs T_J is shown in Figure 3-17.

Thermal runaway will occur when the rate of increase of junction temperature is greater than the rate of increase of ambient temperature. This thermal runaway factor can be expressed by differentiating Equation 3-31 with respect to ambient temperatures.

$$T_R = \frac{dT_J}{dT_A} = \frac{1}{1 - \left[\frac{8350}{(T_J)^2}\ \theta_{JA} S_I V_{CE} I_{CBOTO}\right] \epsilon \left[\frac{(T_J - T_O)\ 8350}{T_J T_O}\right]} \tag{3-32}$$

or

$$T_R = \frac{1}{1 - \frac{8350}{(T_J)^2} \times \theta_{JA} S_I V_{CE} I_{CBOTJ}}. \tag{3-33}$$

Thermal runaway approaches infinity when the denominator approaches zero.

$$T_R = \infty \text{ when } \frac{8350}{(T_J)^2} \times \theta_{JA} S_I V_{CE} I_{CBOTJ} \text{ approaches unity.} \tag{3-34}$$

Therefore to prevent thermal runaway,

$$\theta_{JA} S_I V_{CE} I_{CBOTJ} < \frac{(T_J)^2}{8350}. \tag{3-35}$$

For Motorola industrial power transistors, $T_{J\ max}$ is 100°C or 373°K, and the criteria for thermal runaway is

$$\theta_{JA} S_I V_{CE} I_{CBOTJ} < \frac{373 \times 373}{8350} < 16.7. \tag{3-36}$$

This criteria means that to avoid thermal runaway for a transistor having a maximum $T_J = 100°C$, the product of thermal resistance, current stability factor, collector-to-emitter voltage, and I_{CBO} at 100°C must be less than 16.7.

The allowable ambient temperature would then be calculated by rewriting Equation 3-29 as

$$T_A = T_J - \underbrace{\theta_{JA} I_E V_{CE}}_{\substack{\text{Temperature rise due} \\ \text{to quiescent power}}} - \underbrace{\theta_{JA} S_I V_{CE} I_{CBOTJ}}_{\substack{\text{Temperature rise due} \\ \text{to } I_{CBO} \text{ induced power}}} \tag{3-37}$$

The maximum allowable thermal resistance can then be expressed as

$$\theta_{JA\ max} = \frac{T_{J\ max} - T_{A\ max}}{I_E V_{CE} + S_I V_{CE} T_{J\ max}}. \tag{3-38}$$

If $T_{J\ max} = 100°C$ and the maximum runaway criteria (from Equation 3-36) is inserted into Equation 3-37, a "worst condition" ambient temperature can be determined.

$$T_A = 100 - \theta_{JA} I_E V_{CE} - 16.7 = 83.3 - \theta_{JA} I_E V_{CE}. \tag{3-39}$$

Equation 3-39 states that if the design were based on the worse thermal runaway criteria, then allowable power would be zero at 83.3°C ambient. Thus the "worst condition" thermal resistance must be less than the difference of 83.3°C and the ambient temperature divided by the power dissipation calculated at 25°C. Thus:

$$\theta_{JA\ max} < \frac{83.3 - T_A}{I_E V_{CE}}. \tag{3-40}$$

Thermal runaway will not occur if $\theta_{JA\ max}$ is kept below the limit given in Equation 3-40. Frequently the thermal runaway criteria can be reduced below the 16.7 figure by reducing stability or the applied voltage, thus allowing a higher ambient temperature or greater thermal resistance. In such cases, Equations 3-37 and 3-38 are used. As an example, consider the following problem:

Given: Motorola 2N1531 in a Class A circuit where:

$I_E = 0.5A$

$V_{CE} = 10V$

$T_{A\ max} = 50°C$

$T_{J\ max} = 100°C.$

Permissible change of I_E due to distortion reasons is:
$\Delta I_E = 50$ mA from 25°C ambient
Find: Permissible S_I and θ_{JA} to avoid thermal runaway.

Solution:

$$S_I = \frac{\Delta I_E}{\Delta I_{CBO}}$$

I_{CBO} at $25°C = 0.2 \times 10^{-3}A$

I_{CBO} at $100°C = 12 \times 10^{-3}A$

$$\Delta I_{CBO}\Big]_{25°C}^{100°C} = 11.8 \times 10^{-3}A$$

$$S_I = \frac{50 \times 10^{-3}}{11.8 \times 10^{-3}} = 4.24$$

From Equation 3-40

$$\text{Worst condition } \theta_{JA\ max} < \frac{83.3 - T_A}{I_E V_{CE}} = \frac{83.3 - 50}{5} = 6.66°C/W$$

Thermal runaway criteria

$$S_I V_{CE} \theta_{JA} I_{CBO}\ ]_{100°C} < 16.7$$

$$4.24 \times 10 \times 6.66 \times 12 \times 10^{-3} = 3.38$$

which is less than 16.7 and no runaway will occur.
Since S_I is so low, the worst condition θ_{JA} need not be adhered to and $\theta_{JA\ max}$ can go as high as Equation 3-38 permits:

$$\theta_{JA\ max} = \frac{T_{J\ max} - T_{A\ max}}{I_E V_{CE} + S_I V_{CE} I_{CBOTJ\ max}}$$

$$\theta_{JA\ max} = \frac{100 - 50}{0.5 \times 10 + 4.24 \times 10 \times 12 \times 10^{-3}}$$

$$\theta_{JA\ max} = 9.10°C/W.$$

3-8 — Basic Power Amplifiers (Class A)

Power amplifiers are concerned with one purpose, to deliver a certain amount of power into a load, generally a loud speaker. Obviously an amplifying device used in such applications must have high gain, high efficiency, extended frequency response, and be capable of large power dissipation. A power transistor is such a device.

CLASS A SINGLE-ENDED POWER AMPLIFIERS: Class A single-ended power amplifiers, as defined in Section 3-1, allow 360° of sine wave conduction. A typical common-emitter power stage is illustrated in Figure 3-18.

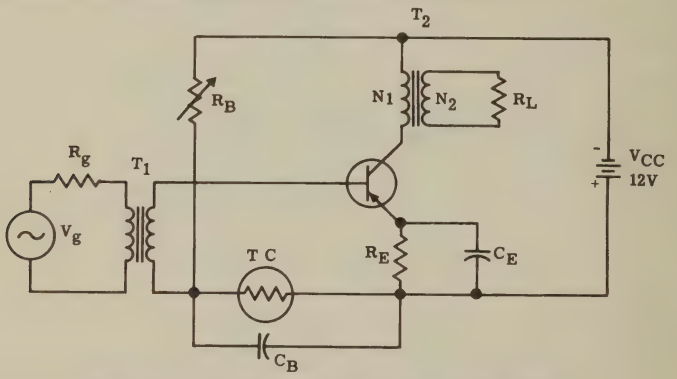


Figure 3-18 — Typical Class A Audio Amplifier

The common emitter connection provides the greatest gain and is most often used. This stage will be analyzed in the succeeding section.

The D-C circuit in Figure 3-18 is the same as Figure 3-7 and the setting of the Q point is as described in Section 3-1. Since the R_E and R_B resistors are now bypassed, the composite characteristic curves for A-C operation will not include their effect and the equivalent A-C circuit will be as shown in Figure 3-19.

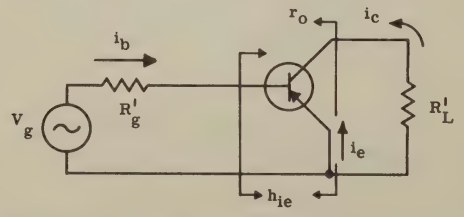


Figure 3-19 — Common Emitter Equivalent AC Circuit

In the A-C equivalent circuit, R'_g includes the D-C resistance of the transformer and the equivalent bias network plus the transformed value of the generator resistor, R_g, looking back into the secondary of the driver transformer, T_1. The value of R'_L is the transformed value of the load resistance looking into the primary of the output transformer, T_2.

POWER GAIN: Analysis of the circuit in Figure 3-18 will show that the power output is limited by the voltage and the load resistors. This analysis results in Equations 3-41 and 3-42 which apply up to the point of signal clipping, assuming $V_{C\,sat}$ and I_{CBO} to be negligible. Also see Figure 3-20.

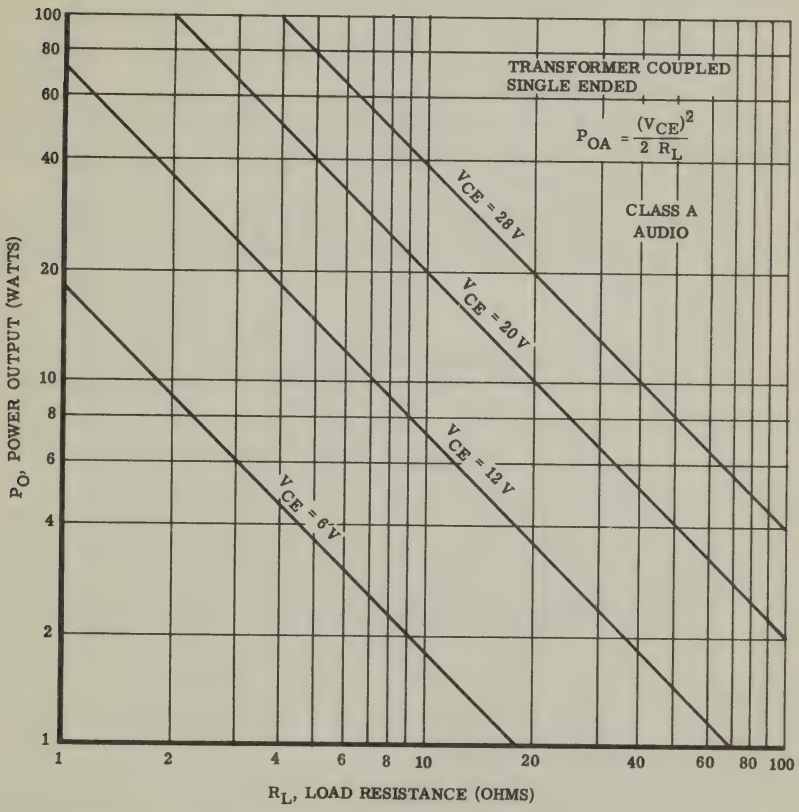


Figure 3-20 — Single Ended Power Output — Load Resistance Nomograph

$$P_o = i_c^2 R'_L \tag{3-41}$$

$$P_{o\,max} = \frac{(V_{CC})^2}{2R'_L} \tag{3-42}$$

where i_c is rms collector current and V_{CC} is D-C collector supply voltage.

Considering the output transformer, T_2:

$$P_{o\ max} = \left(\frac{N_2}{N_1}\right)^2 \times \frac{(V_{CC})^2}{2R'_L}. \tag{3-43}$$

Input power to a stage is:

$$P_i = (i_b)^2\,(R'_g + h_{ie}) \tag{3-44}$$

Assuming $h_{ie} << R_B$, power gain, G_s, of the stage is:

$$G_s = \frac{P_o}{P_i} = \frac{i_c{}^2 R'_L}{i_b{}^2(R'_g + h_{ie})} = \frac{(h_{fe})^2 R'_L}{R'_g + h_{ie}} \tag{3-45}$$

Maximum stage power gain will occur when R'_g is zero and maximum power transfer occurs when $R'_g = h_{ie}$.

Maximum stage power gain at maximum power transfer

$$G'_s = \frac{(h_{fe})^2 R'_L}{2h_{ie}} \tag{3-46}$$

Usually no attempt is made to match the load resistance, R_L, to the transistor output resistance, r_o, because the load is completely dependent upon power level and available supply voltage.

COMMON EMITTER CONNECTION: A correlation between h_{fe} and h_{ie} in power transistors can be seen in the simple equivalent circuit of the input shown in Figure 3-21.

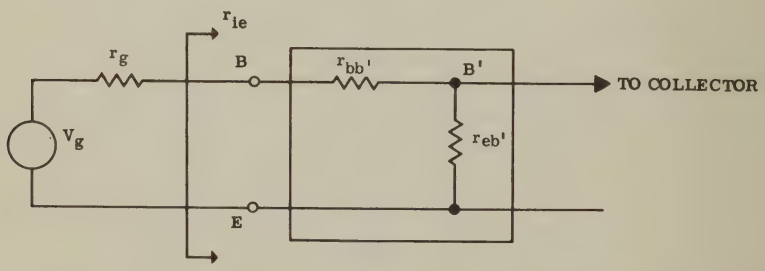


Figure 3-21 — Equivalent AC Transistor Input Circuit

From Figure 3-21, the input resistance, r_{ie}, may be developed:

$$r_{ie} \approx h_{ie} \approx r_{bb'} + h_{fe} r_{eb'} \tag{3-47}$$

Thus transistor power gain may be written

$$G_e = \frac{(h_{fe})^2 R'_L}{r_{bb'} + h_{fe} r_{eb'}} \tag{3-48}$$

Combining Equations 3-47 and 3-48

$$G_e = \frac{(h_{fe})^2 R'_L}{h_{ie}}. \tag{3-49}$$

Since

$$g_{fe} = \frac{h_{fe}}{h_{ie}}, \tag{3-50}$$

$$G_e = (h_{fe})(g_{fe}R_L). \tag{3-51}$$

Power Gain = (Current gain (Voltage gain)

The correlation of h_{ie}, h_{FE}, and G_e for one group of Motorola power transistors has been plotted along with a frequency cutoff correlation line in Figure

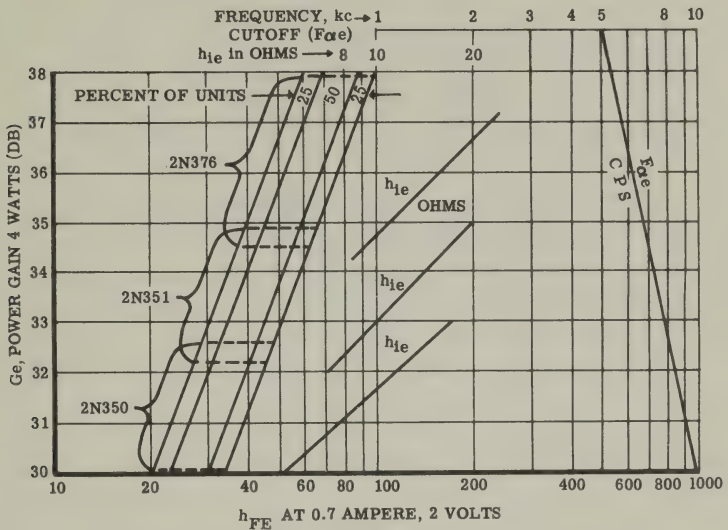


Figure 3-22 — Typical Relation of G_e, h_{fe}, h_{ie}, and $F_{\alpha e}$

COMMON-BASE CONNECTION: Common-base connection requires that the signal be fed into the emitter as shown in Figure 3-23. Input current very nearly equals output current because the current gain is near unity.

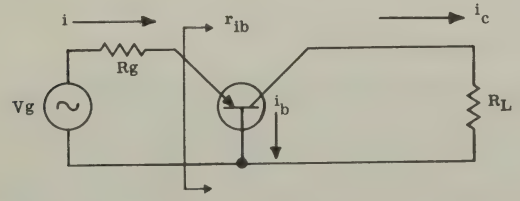


Figure 3-23 — Common Base

The input resistance is:

$$r_{ib} \approx h_{ib} \approx r_{eb}' + \frac{r_{bb}'}{h_{fe}}, \tag{3-52}$$

and power gain is

$$G_b = \frac{(h_{fb})^2 R_L}{r_{eb}' + \frac{r_{bb}'}{h_{fe}}} = \frac{(h_{fb})^2 R_L}{r_{ib}}. \tag{3-53}$$

Because $h_{fb} \approx 1$, $(h_{fb})^2 \approx 1$. Also

$$r_{ib} \approx h_{ib} \approx \frac{h_{ie}}{h_{fe}} = \frac{1}{g_{fe}}. \tag{3-54}$$

Thus Equation 3-53 can be rewritten

$$G_b = g_{fe} R_L. \tag{3-55}$$

The power gain of the common base configuration is then equal to the voltage gain portion of the common-emitter equation (3-51).

COMMON COLLECTOR: Similar arguments hold for common-collector circuits where voltage gain is nearly unity. Thus for the circuit of Figure 3-24, input resistance and power gain are:

$$r_{ic} \approx h_{ie} + (h_{fe} + 1)\, R_L \approx h_{fe} R_L, \tag{3-56}$$

and

$$G_c = h_{fe} \tag{3-57}$$

which is the current gain portion of the common emitter equation 3-51.

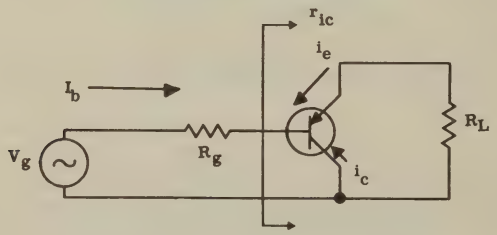


Figure 3-24 — Common Collector

3-9 — Distortion (Class A)

The distortion of a Class A-biased amplifier is theoretically zero but due to nonlinear characteristics of the transistor, a certain amount of distortion exists. Distortion can be minimized in common-emitter circuits by driving the base from a low source impedance, as illustrated in Figure 3-25. The usual practice is to match the driving impedance with the transistor input impedance for maximum power gain. This level (10-30 ohms) results in low distortion. Distortion versus source impedance is shown in Figure 3-26 for a typical 2N176 Motorola power transistor at 2 watts output power, with $h_{ie} \approx 15$ ohms.

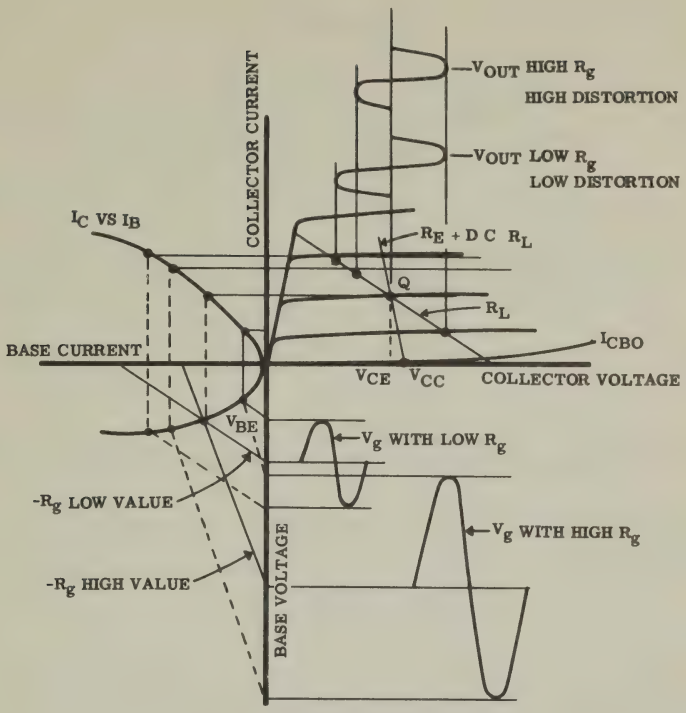


Figure 3-25 — Effect of Source Resistance Upon Distortion

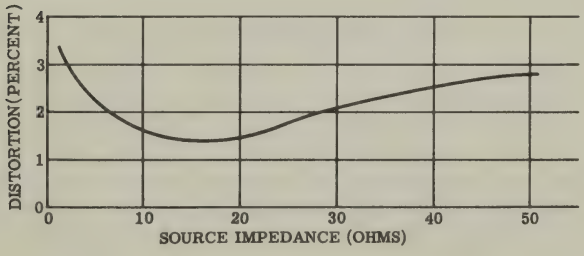


Figure 3-26 — Distortion Versus Source Impedance for 2N176

3-10 — Efficiency (Class A)

The maximum efficiency of a transformer-coupled Class A stage occurs at maximum output power and cannot exceed 50% for pure sine wave operation. The efficiency is a direct function of power output.

Current and voltage waveforms are shown in Figure 3-27.

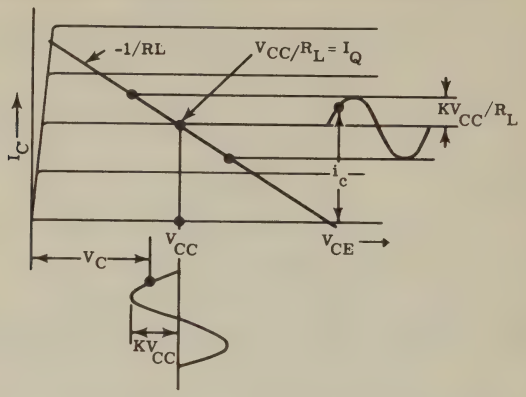


Figure 3-27 — Relation of DC Collector Voltage and Current to AC Voltage and Current

The power dissipated in the device will be the time integral of the transistor current and voltage.

$$P_d = \frac{1}{2\pi}\int_0^{2\pi} v_c i_c \, dt, \tag{3-58}$$

where

$$v_c = V_{CC} - KV_{CC} \sin \omega t, \tag{3-59}$$

$$i_c = \frac{V_{CC}}{R_L} + \frac{KV_{CC}}{R_L} \sin \omega t, \tag{3-60}$$

P_d = power dissipated in the transistor, and

K = a proportional constant from 0 to 1 depending on the voltage output level. K is defined as the ratio of the peak signal voltage divided by V_{CC}:

$$K = \frac{V_p}{V_{CC}}. \tag{3-61}$$

Thus:

$$P_d = \frac{1}{2\pi}\int_0^{2\pi} \left[\frac{(V_{CC})^2}{R_L} + \frac{K^2 (V_{CC})^2}{R_L} \sin^2 \omega t\right] d\omega t \tag{3-62}$$

$$P_d = \frac{(V_{CC})^2}{R_L} - \frac{K^2 (V_{CC})^2}{2R_L}. \tag{3-63}$$

The output power delivered to the load at any level will be:

$$P_o = \frac{K^2 V_{CC}^2}{2R_L}. \tag{3-64}$$

The power supplied from the battery (P_{DC}) must equal the power dissipated in the transistor plus the load power:

$$P_{DC} = P_d + P_o, \text{ or} \tag{3-65}$$

$$P_d = P_{DC} - P_o. \tag{3-66}$$

From Equations 3-63 to 3-65,

$$P_{DC} = \frac{V_{CC}^2}{R_L} \tag{3-67}$$

or from Figure 3-27,

$$P_{DC} = V_{CC} I_Q. \tag{3-68}$$

This D-C power from the battery is independent of the signal power. The efficiency is defined as output power divided by supply power;

$$\eta = \frac{P_o}{P_{DC}}, \tag{3-69}$$

$$\eta = \frac{P_o}{P_d + P_o}, \tag{3-70}$$

$$\eta = \frac{1}{1 + \frac{P_d}{P_o}}. \tag{3-71}$$

By combining Equations 3-63, 3-64 and 3-71, Class A efficiency, η, becomes

$$\eta = \frac{K^2}{2}. \tag{3-72}$$

Since both efficiency and power output varies as K^2, the relation of η to P_o is linear. At maximum power output, K will equal unity and the best Class A efficiency will be 0.5 or 50%. Actual efficiency cannot reach 50% because of saturation voltage at peak current.

The peak current equals

$$I_p = \frac{2V_{CC} - V_{CE\,sat}}{R_L}. \tag{3-73}$$

3-11 — Push-Pull Amplifiers (Class A, AB, and B)

Because of the efficiency limitations of single-ended Class A operation, the more efficient push-pull Class AB circuit is often used at high power levels. Push-pull is also attractive from output transformer considerations. It permits reduction of core size because the D-C currents in each half of the primary winding tend to cancel each other's effect on core saturation flux. A typical push-pull circuit is shown in Figure 3-28. The A-C output equivalent circuits for

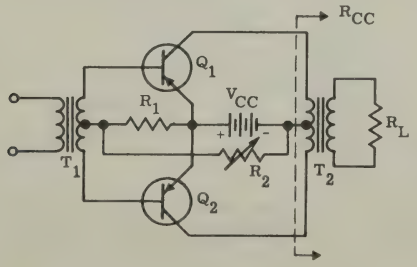


Figure 3-28 — Push-Pull Schematic

Class B and Class A are shown in Figures 3-29 and 3-30.

The effects of adjusting the bias to obtain the desired class of operation in push-pull arrangements can best be illustrated by examining the composite transconductance transfer characteristic curves in Figures 3-31 and 3-32.

Figure 3-31 shows that pure Class B operation will have a cross-over distortion effect in the output wave shape due to the nonlinearity of the transconductance curve. The current gain I_C versus I_B curve will show similar effects. With Class B operation the composite static curves are identical with the dynamic curves. To eliminate the cross-over distortion in the dynamic curves, a forward bias is applied. This has the effect of sliding the lower curve, Q_2, to the right. The static curves for each transistor are still the same. However, both bases share the same forward voltage bias because with transformer coupling the base to emitter junctions of Q_1 and Q_2 are effectively in parallel. The composite dynamic V_{BE}-I_C curve is the sum of the two static curves added together in the current direction.

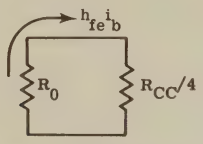


Figure 3-29 — Class B Push-Pull Output Equivalent Circuit

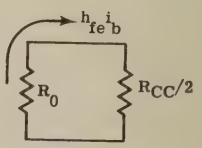


Figure 3-30 — Class A Push-Pull Output Equivalent Circuit

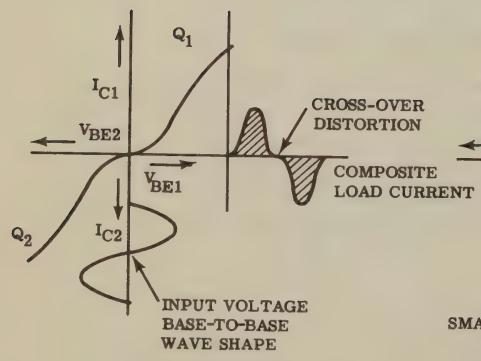


Figure 3-31 — Class B Push-Pull Composite V_{BE}-I_C Curve

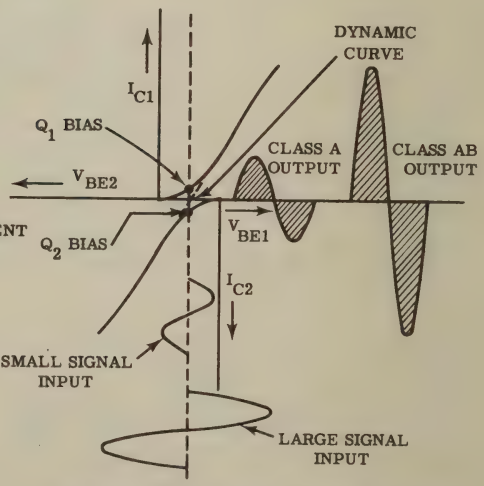


Figure 3-32 — Class A and AB Push-Pull Composite V_{BE}-I_C Curve

For small signals both transistors conduct for the full 360° as in single-ended Class A operation. The total collector output current for small signals is the sum of the output current of the individual transistors. Distortion cancellation is comparable to single-ended use since the composite dynamic curve is much more linear at small signals than curves of the individual transistors, which are very nonlinear.

With large-signal input the operation becomes essentially Class B. If large-signal Class A operation is desired, the bias is increased and the dynamic composite curve applies over a larger range.

Graphical analysis of the input and output characteristics helps explain certain aspects of push-pull operation. For instance, the composite input curve shown in Figure 3-33 is similar to the curve for transconductance.

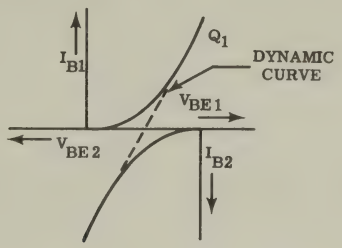


Figure 3-33 — Composite Dynamic Push-Pull Input Curve

The composite output characteristic curve is shown in Figure 3-34, which illustrates an inverted output characteristic for one of the transistors, Q_2. The output characteristics of the two transistors share a common point at the battery potential V_{CC}. The load lines for the various classes of operation are indicated on the composite curve. The composite dynamic load line extends from I_{P1} to

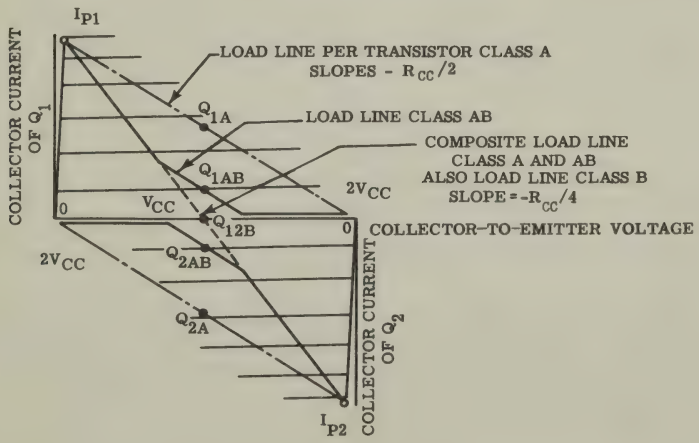


Figure 3-34 — Composite Push-Pull Output Characteristic

I_{P2}, passing through V_{CC}. It is the same regardless of the class of operation. However, the load line for each transistor varies considerably with bias and exerts a considerable effect on gain. These load lines can be observed very easily on an oscilloscope by the insertion of a current-sensing resistor in series with one collector. When operating Class B, the dynamic composite line, $R_{cc}/4$, is also the individual transistor load line. With Class A operation the load resistance per transistor, $R_{cc}/2$, is represented by the dashed line and is equal to twice the Class B load resistance. When operating Class AB the load resistance per transistor shifts from the Class A value at low signals to the Class B value at large signals for half the wave and becomes infinite (the horizontal portion) during the cutoff portion of the wave shape.

The manner in which maximum output is related to V_{CC} and load resistance can best be demonstrated by assuming perfect transformers. It can be shown that the equivalent collector-to-collector resistance, regardless of class of operation, is:

$$R_{cc} = \left(\frac{2N_1}{N_2}\right)^2 R_L . \tag{3-74}$$

The maximum power output per transistor during its conduction will be equal to the rms value of V_{CC} squared, divided by the load resistance per transistor, or

$$P_{o\ max} = \frac{V_{CC}^2}{2R'_L} . \tag{3-75}$$

With Class B operation

$$R'_{LB} = \frac{R_{cc}}{4} . \tag{3-76}$$

A single transistor see one-fourth of the total collector-to-collector resistance. This effect is due to the 2:1 turns ratio of the transformer primary which gives a 4:1 impedance ratio. The R'_{LB} is the composite dynamic load line of Figure 3-34.

For Class A operation

$$R'_{LA} = \frac{R_{cc}}{2} . \tag{3-77}$$

Equations 3-76 and 3-77 are illustrated by the composite output curve. Thus maximum Class B power output is

$$P_{oB\ max} = \frac{2V_{CC}^2}{R_{cc}} . \tag{3-78}$$

Note that both the total and the individual transistor power during its 180° conduction interval are the same as the maximum Class B power output. Average power output per transistor for 360° would be half this value. Class B power output curves are shown in Figure 3-35.

Class A power output per transistor is

$$P'_{oA\ max} = \frac{V_{CC}^2}{R_{cc}} . \tag{3-79}$$

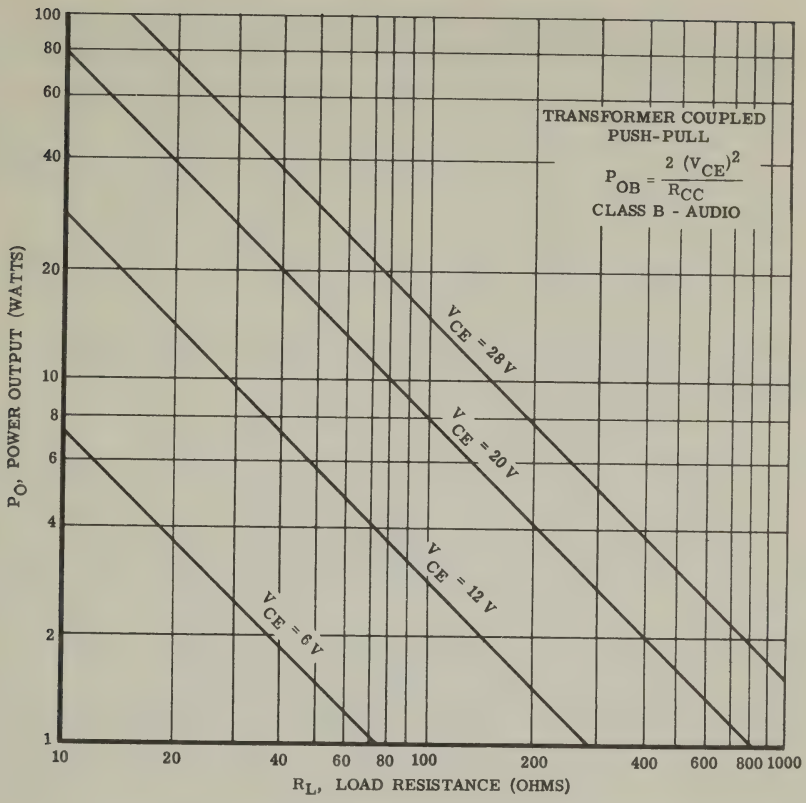


Figure 3-35 — Push-Pull Power Output — Load Resistance Nomograph

Since both transistors operate 360° in Class A operation, the power is additive in the load.

Thus, total maximum Class A power output is

$$P_{oA\ max} = \frac{2V_{CC}^2}{R_{cc}}. \tag{3-80}$$

Therefore the maximum power output for Class A operation and Class B operation is the same. Then the maximum power output for push-pull operation is

$$P_{oPP\ max} = \left(\frac{N_2}{N_1}\right)^2 \times \frac{(V_{CC})^2}{2R_L}. \tag{3-81}$$

Maximum push-pull power output is similar to the Class A single-ended Equation 3-43 except that N_1 in the push-pull case has half the number of total primary turns.

Also with pure Class B push-pull the actual power output will usually be somewhat lower than the theoretical power because of the cross-over portion which eliminates part of the useful conduction:

PUSH-PULL INPUT RESISTANCE: The input resistance of transformer-coupled push-pull stages is complicated somewhat by the nonlinearity of V_{BE} versus I_B. The following equations, however, are close to the true values:

For Class A operation

$$R_{in} \approx h_{ie}, \text{ and} \tag{3-82}$$

$$R_{bb} \approx 2h_{ie}. \tag{3-83}$$

For Class B operation

$$R_{in} \approx h_{ie}, \text{ and} \tag{3-84}$$

$$R_{bb} \approx 4h_{ie}. \tag{3-85}$$

PUSH-PULL POWER GAIN: Power gain relationships can be developed in the same manner as the single-ended relationships.

For both Class A and B operation

$$G_e = \frac{(h_{fe})^2 R_{cc}}{R_{bb}}. \tag{3-86}$$

Class A —

$$G_{eA} = \frac{(h_{fe})^2 R_{cc}}{2h_{ie}} \tag{3-87}$$

Class B —

$$G_{eB} = \frac{(h_{fe})^2 R_{cc}}{4h_{ie}} \tag{3-88}$$

Therefore, Class A push-pull operation will theoretically result in twice the power gain of Class B operation. This means power gain will vary with power output in Class AB operation. Also current gain drops as collector current increases and all classes of operation show a loss in power gain at high power levels.

3-12 — Push-Pull Distortion

If the relation of base-emitter voltage to collector current were perfectly linear, a single-ended Class A stage would have zero harmonic distortion. This is also true for Class A push-pull. But linearity may not eliminate harmonic distortion in Class B or Class AB push-pull operation.

Consider two transistors, chosen with perfectly linear V_{BE} versus I_C curves but with different transconductances. This condition is shown graphically in Figure 3-36. In the special case where the slopes of the two devices are equal there will be no distortion. In practice, transistors do not have linear characteristics; however, matching of both current gain and transconductance will reduce the large signal distortion in Class B push-pull. Also if the matching is perfect all even order harmonics will be canceled.

There would be little use for Class AB operation if the hypothetical linearity were possible since increased distortion would result even if matched units were used. This distortion effect is shown in Figure 3-37.

The actual transconductance curve (and sometimes the current gain) will be very nonlinear at low collector currents and will asymptotically approach a

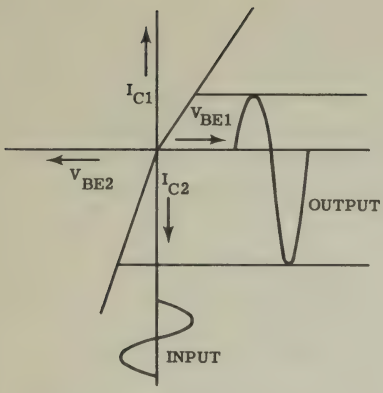


Figure 3-36 — Class B Push-Pull Transconductance Dynamic Curve Showing Effect of Mismatch

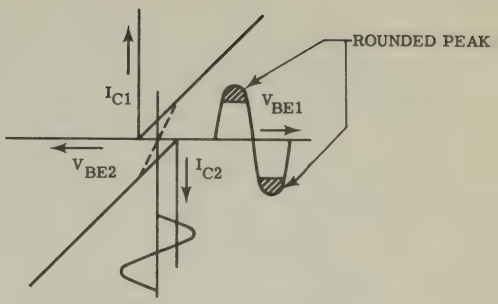


Figure 3-37 — Class AB Push-Pull Operation of Linear Transistor

straight line function for a large part of its useful range. Thus with carefully matched devices, very low distortion is possible with Class AB operation, as shown in Figure 3-32.

In actual circuits the resistances of the generator and bias network frequently can be optimized to improve over-all linearity although at a sacrifice in gain. For instance, employing the common-collector configuration (emitter follower) will usually decrease distortion. If the load impedance for the emitter follower is a pure resistance it will swamp out the transistor nonlinearities. This type of linear operation is discussed in Section 3-18 on the design of a 10-watt amplifier.

3-13 — Push-Pull Circuit Efficiency

Efficiency of a Class A push-pull stage is a linear function of power output and is equal to the efficiency of a Class A single-ended stage, namely 50% maximum at maximum power output. However the Class B efficiency is not a linear function, as shown by the following analysis: The collector current wave shape per transistor is a half-wave pulse and the voltage wave shape a sine wave. This combination results in a power wave shape similar to that in Figure 3-38.

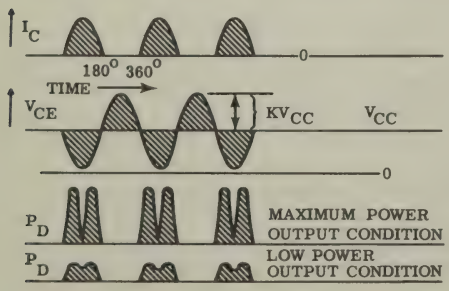


Figure 3-38 — Class B Push-Pull Collector Current, Voltage and Power Dissipation Waveshapes

The power pulses have a frequency component double that of the voltage frequency. The peak of the power pulses varies directly with the output voltage level, whereas the valley between the pulses varies inversely as the output voltage. This variation in power distribution throughout the conduction period has the effect of increasing the power dissipation as output power is decreased from maximum until a peak is reached at the power level equal to four-tenths of the maximum power output.

The power dissipated in each transistor for the full cycle is

$$P_d = \frac{1}{2\pi} \int_0^{\pi} (V_{CC} - KV_{CC} \sin \omega t) \left(\frac{KV_{CC}}{R'_{LB}} \sin \omega t \right) d\omega t, \qquad (3\text{-}89)$$

or

$$P_d = \frac{KV_{CC}^2}{\pi R'_{LB}} \left[1 - \frac{K\pi}{4} \right]. \qquad (3\text{-}90)$$

The efficiency is

$$\eta = \frac{1}{1 + \frac{P_d}{P_o}}, \qquad (3\text{-}91)$$

where P_d is the power dissipated by each transistor for the full cycle and P_o is the average power delivered to the load by each transistor for the full cycle.

Class B output power for each transistor at any level is

$$P_o = \frac{(KV_{CC})^2}{4R'_{LB}} \text{ per full cycle.} \qquad (3\text{-}92)$$

From Equations 3-90, 3-91 and 3-92

$$\eta_{PP\,max} = \frac{K\pi}{4}. \qquad (3\text{-}93)$$

Because maximum efficiency results with $K = 1$, which is when peak signal voltage equals V_{CC},

$$\eta_{PP\,max} = \frac{\pi}{4} = 78.5\%. \qquad (3\text{-}94)$$

Class B push-pull efficiency is directly proportional to the voltage level in the output signal, but does not vary directly with power out. Thus a plot of efficiency against power output will be similar to that of Figure 3-39, where efficiency, $\eta_{PP\,max}$, is plotted against the ratio of power out to the maximum power output (K^2).

The maximum dissipation within each transistor can be obtained by combining Equations 3-90 and 3-92 and expressing the power dissipation in terms of power output and some constants. Setting power output $dP_d/dP_o = 0$, will result in the values of P_d and P_o, where P_d is a maximum.

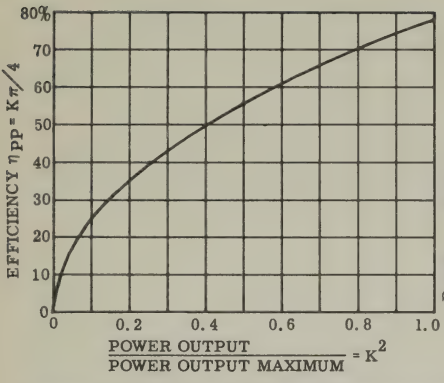


Figure 3-39 — Class B Push-Pull Efficiency as a Function of Output Power

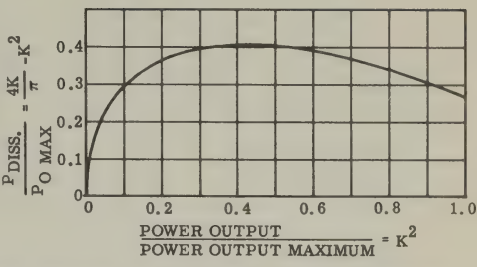


Figure 3-40 — Class B Push-Pull Power Dissipated as a Function of Power Output

Combining Equations 3-90 and 3-92 yields

$$P_d = \frac{2V_{CC}\sqrt{P_o}}{\pi\sqrt{R'_{LB}}} - P_o. \tag{3-95}$$

Differentiating Equation 3-95 yields

$$\frac{dP_d}{dP_o} = \frac{V_{CC}}{\pi\sqrt{R'_{LB}}\sqrt{P_o}} - 1. \tag{3-96}$$

Maximum dissipation occurs when this expression equals 0.
Where P_d is maximum

$$P_o = \frac{(V_{CC})^2}{\pi^2 R'_{LB}}. \tag{3-97}$$

Substituting Equation 3-97 in Equation 3-95:

$$P_{d\ max} = \frac{(V_{CC})^2}{\pi^2 R'_{LB}}. \tag{3-98}$$

Therefore at maximum power dissipation $P_o = P_{d\ max}$ and the efficiency, η, = 50%.

This maximum dissipation occurs when

$$K = \frac{2}{\pi}, \tag{3-99}$$

and the output power is

$$P_o = \frac{4}{\pi^2} P_{o\ max}, \tag{3-100}$$

or

$$P_o \approx 0.4 P_{o\,max} \tag{3-101}$$

at the maximum dissipation, as shown in Figure 3-40.

The peak current for push-pull operation is the same for either Class A or B:

$$I_{peak} = \frac{4V_{CC}}{R_{CC}}. \tag{3-102}$$

3-14 — Amplifier Design Procedures

The design of audio amplifiers requires a logical approach and the making of certain arbitrary decisions. The following points have proved useful in outlining design program requirements.

I. **Ideal Design Case**

A. Approximate an ideal design by assuming perfect transistors, base the design upon typical gain, and so forth.

B. Solve for load resistance, power gain, collector peak voltage, and "Q" point from maximum power output requirements and convenient supply voltage.

II. **Actual Design Case**

(Based on values obtained in the ideal design case.)

A. Set up a general bias network, establishing values where practical (see Section 3-3). In single-ended Class A, set R_E such that nominal $I_C \times R_E$ is in the 0.5 V to 1.0 V range.

B. Establish a practical load line based on R_E, R_C, transistor saturation resistance ($R_{C\ sat}$), and transformer losses. The design center load resistance will not allow clean output with all variations. Thus, a lower resistance must be assumed. A practical method is to design for a 50% increase in power output for Class A and 25% for Class B which allows for various losses. Thus . . .

Class A

$$R'_L = \frac{(V_{CC})^2}{3P_{o\ max}}, \tag{3-103}$$

and

Class B

$$R_{CC} = \frac{2(V_{CC})^2}{1.25P_{o\ max}}. \tag{3-104}$$

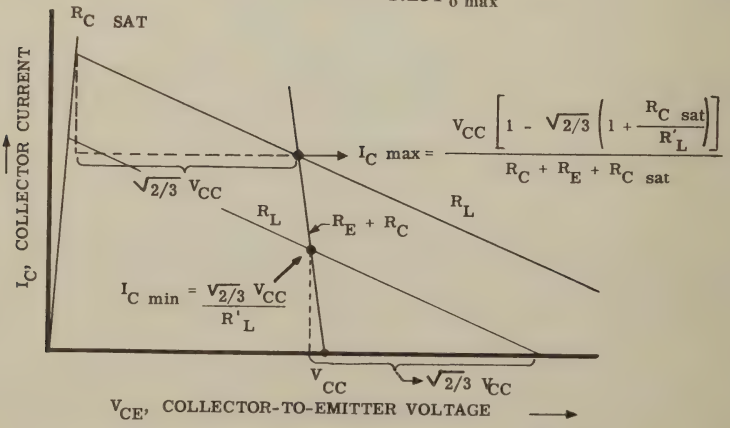


Figure 3-41 — Graphical Method to Find $I_{C\ max}$ and $I_{C\ min}$

C. From Figure 3-41, the following equations can be developed:

$$I_{E\,max} = \frac{V_{CC}\left[1 - \sqrt{2/3}\left(1 + \frac{R_{C\,sat}}{R'_L}\right)\right]}{R_C + R_E + R_{C\,sat}},$$

which, when $R_{C\,sat}$ is much smaller than R'_L, reduces to

$$I_{E\,max} = \frac{0.19V_{CC}}{R_C + R_E + R_{C\,sat}} \tag{3-105}$$

$$I_{E\,min} = \frac{\sqrt{2/3}\,V_{CC}}{R'_L}. \tag{3-106}$$

DESIGN EXAMPLE

Class A single-ended, transformer-coupled

$V_{CC} = 12V$

$P_{o\,max} = 2W$

T_A range 25°C - 40°C

I. **Ideal Case**

$$R_L = \frac{V_{CC}^2}{2P_{o\,max}} = \frac{(12)^2}{2 \times 2} = 36 \text{ ohms}$$

$$I_C = \frac{V_{CC}}{R_L} = \frac{12}{36} = 333 \text{ mA}$$

$$V_{peak} = 2V_{CC} = 2 \times 12 = 24V$$

A Motorola 2N176 power transistor is chosen.

Nominal $h_{fe} = 45$

$h_{ie} = 16$

$$G_e = \frac{(h_{FE})^2 R_L}{h_{ie}} = \frac{(45)^2\,36}{16} = 4650$$

$$= 10 \log 4650 = 36.7 \text{ db}$$

$$\text{Power in} = \frac{P_o}{G_e} = \frac{2}{4650} = 0.43 \text{ mw}.$$

II. **Actual Case**

Assume 0.5V across R_E at 500 mA; then $R_E = 1\Omega$.
Assume output transformer DC resistance $R_C = 1\Omega$.
$R_{C\,sat}$ from 2N176 data sheet is about 0.5Ω.

$$I_{E\,max} = \frac{0.19V_{CC}}{R_C + R_E + R_{C\,sat}} = \frac{0.19 \times 12}{1 + 1 + 0.5} = 912 \text{ mA}$$

$$I_{E\,min} = \frac{2/3\,V_{CC}}{R'_L} = \frac{0.81 \times 12}{24} = 405 \text{ mA}.$$

An $I_{E\,max}$ of 912 mA is somewhat excessive, and a value of 600 mA would be more practical. To establish these values, a bias network is established (see Section 3-3).

3-15 — Miscellaneous Circuits

Variations upon the classical single-ended and push-pull circuits continue to be evolved. Some of these are reproduced in Figures 3-42 through 3-47.

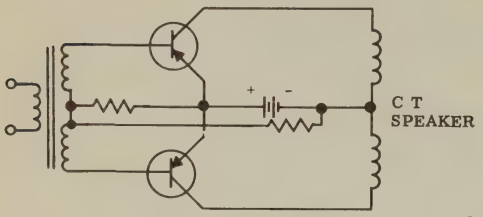


Figure 3-42 —
Center Tab Speaker Push-Pull

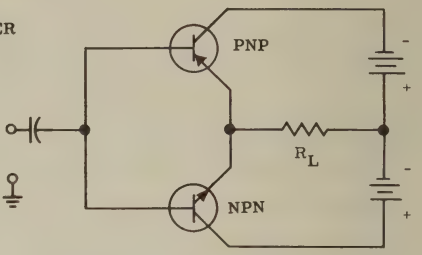


Figure 3-43 — Complementary

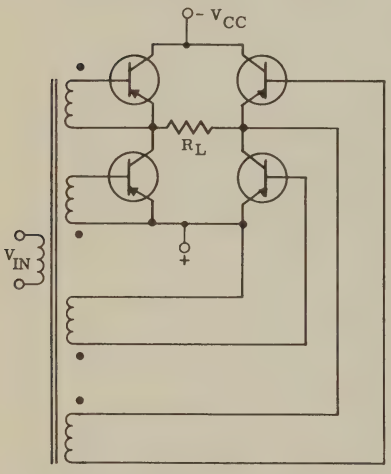


Figure 3-44 — Bridge

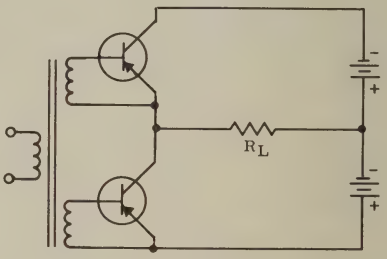


Figure 3-45 — Half Bridge
with Split Power Supply

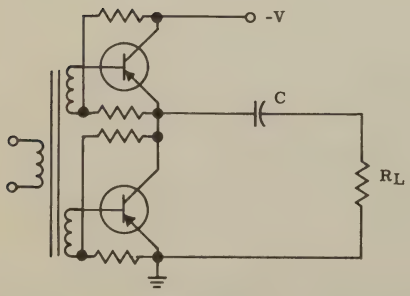


Figure 3-46 —
Half Bridge Cap. Coupled Load

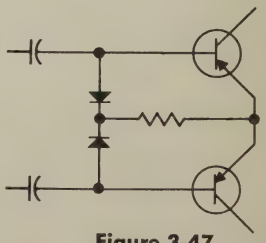
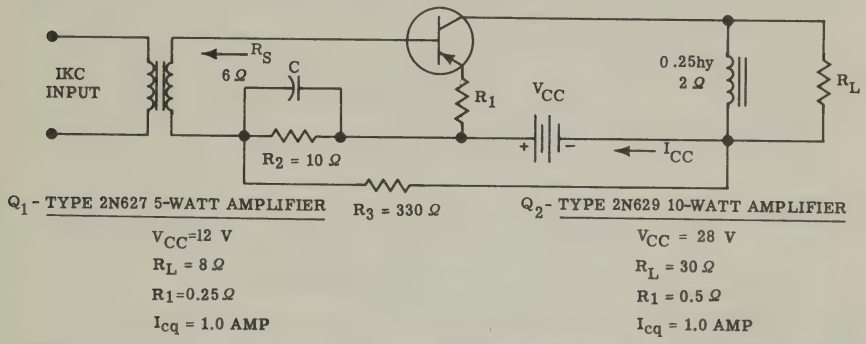


Figure 3-47 —
R.C. Coupling with Diodes

3-16 — Amplifier Applications

In this section typical Class A and push-pull Class B power stages will be discussed. Motorola types 2N627 and 2N629 were used for the measurements described.

Figure 3-48 shows a typical single-ended circuit. The emitter resistor, R_1, provides emitter degeneration which greatly improves stability and lowers distortion. Biasing is accomplished by use of resistors R_1, R_2, and R_3. A bypass capacitor, C_1, prevents loss of signal in the bias network. If a wide temperature range will be encountered, one of these resistors could be replaced by a thermistor, or some of the more sophisticated bias arrangements previously described could be used. The impedance which the base sees should be low to allow full use of the linear transconductance of Motorola power transistors. In this case, a 6-ohm source resistance proved optimum.



Q_1 - TYPE 2N627 5-WATT AMPLIFIER — R_3 = 330 Ω — Q_2 - TYPE 2N629 10-WATT AMPLIFIER

V_{CC}=12 V	V_{CC} = 28 V
R_L = 8 Ω	R_L = 30 Ω
R_1=0.25 Ω	R_1 = 0.5 Ω
I_{cq} = 1.0 AMP	I_{cq} = 1.0 AMP

Figure 3-48 — Series Transistors with Transformer Input and Capacitor Output

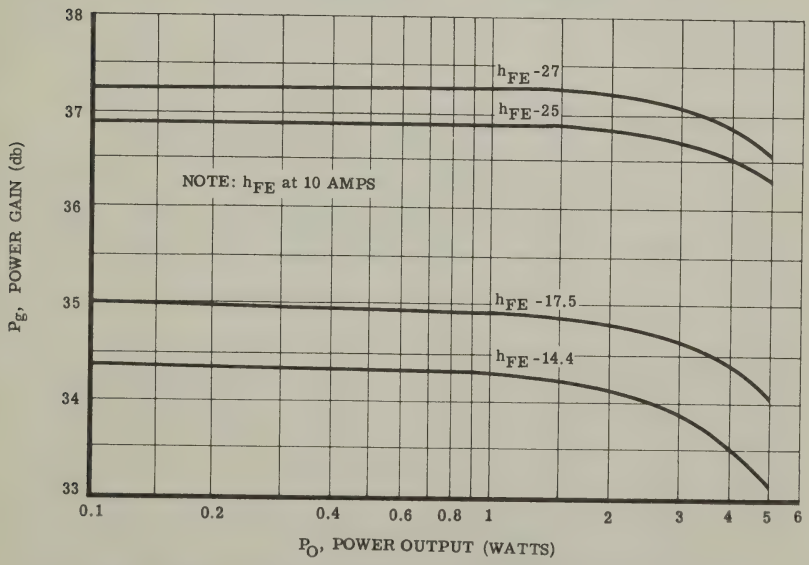


Figure 3-49 — Power Gain Versus Power Output (5 Watt Amplifier)

Figures 3-49 and 3-50 show the performance of a 5-watt amplifier using a 12-volt supply. Figures 3-51 and 3-52 show the performance of a 10-watt amplifier using a 28-volt supply. The families of curves were obtained by using transistors having different D-C current gains. The current gain was measured at 10 amperes. As might be expected, the higher gain devices show higher power gain and less variation in gain with power output. This effect is reflected in the distortion curves which show lower values for the high-gain transistors.

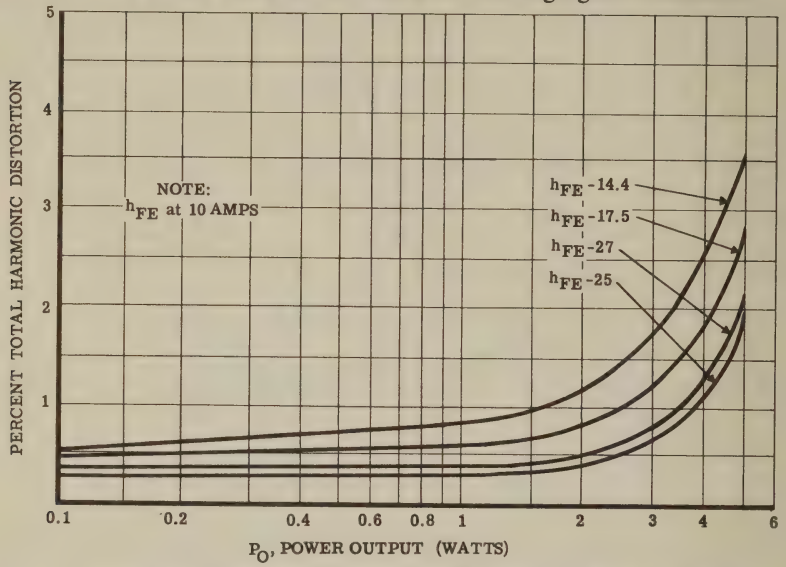


Figure 3-50 — Distortion Versus Power Output (5 Watt Amplifier)

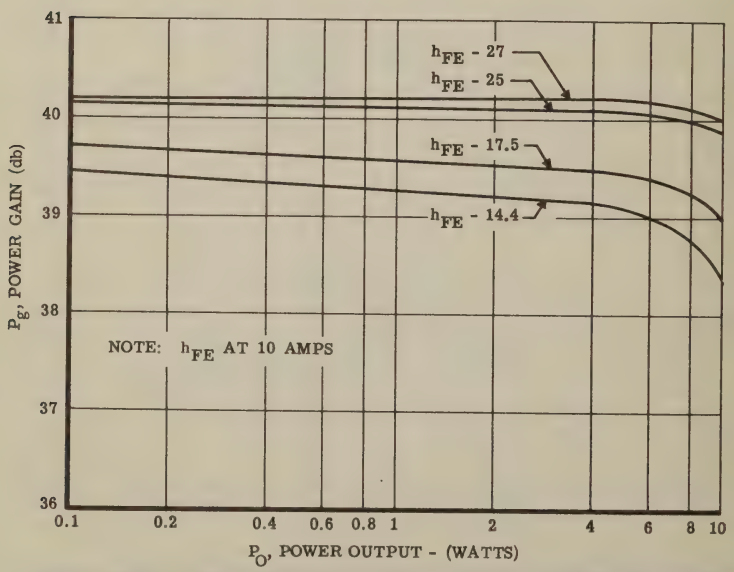


Figure 3-51 — Power Gain Versus Power Output (10 Watt Amplifier)

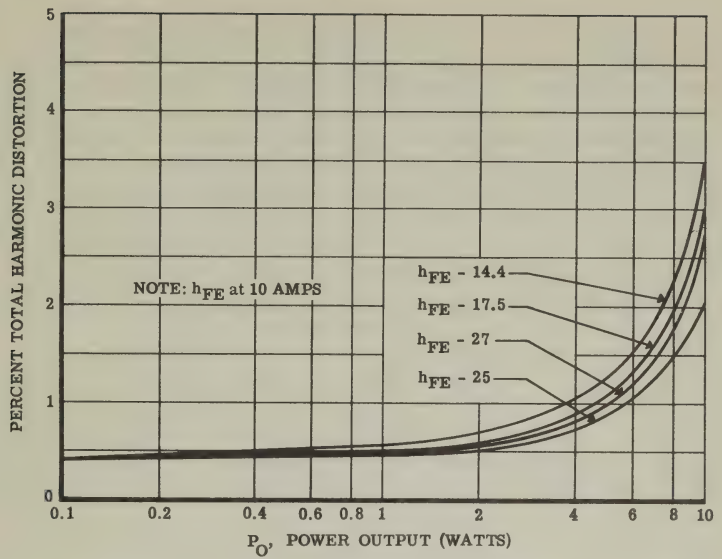
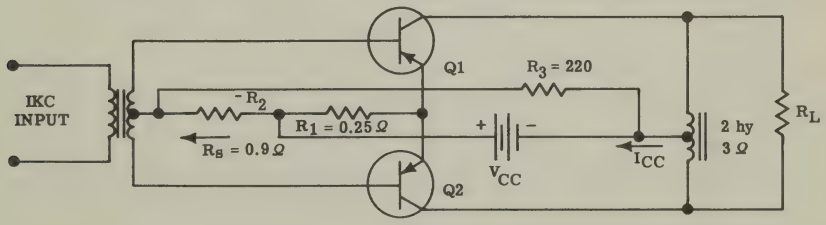


Figure 3-52 — Distortion Versus Power Output (10 Watt Amplifier)

The schematic of the push-pull Class B amplifier is shown in Figure 3-53. The function of the resistors is the same as in the single-ended amplifier. Here the very low source resistance of 0.9 ohm must be used to minimize distortion, largely because of current gain nonlinearity in the very low current gain region. Performance curves for the 10-watt amplifier using a 12-volt supply are shown in



TYPE 2N627 10-WATT AMPLIFIER	TYPE 2N629 25-WATT AMPLIFIER
V_{CC} = 12 VOLTS	V_{CC} = 28V
R_L = 15 Ω	R_L = 40 Ω
R_2 = 3 Ω	R_2 = 1 Ω
I_{cq} = 0.1 AMP	I_{cq} = 0.2 AMP
I_{cm} = 1.5 AMPS	I_{cm} = 1.7 AMPS

Figure 3-53 — 10-25 Watt Class B Amplifier Circuit

Figures 3-54 and 3-55; data for the 25-watt amplifier operating from a 28-volt supply is shown in Figures 3-56 and 3-57. Note the importance of matching the current gain. Actually since this amplifier is essentially voltage driven, the transconductance of the push-pull pairs should be matched in order to obtain minimum distortion. Transconductance should also track over the current operating range, but a match at low current and at maximum current will usually suffice. Use of emitter resistors will make the matching problem less critical.

This amplifier does not operate in true Class B since the transistors must be operated at projected cutoff in order to minimize crossover distortion. Even so, some crossover distortion still persists as evidenced by the rise in distortion at very low levels. Careful matching and/or over-all negative feedback can be used to reduce this distortion to an acceptable level.

It should be mentioned that the generator used for these measurements had a measured distortion of 0.3%. Another point bears emphasizing. Since the common-emitter transfer characteristic of a power transistor is more linear when driven from a low impedance source, matching to the source for maximum gain is generally not done. In the case of the push-pull amplifier described, an emitter follower circuit or some other feedback amplifier will generally be required for the driver.

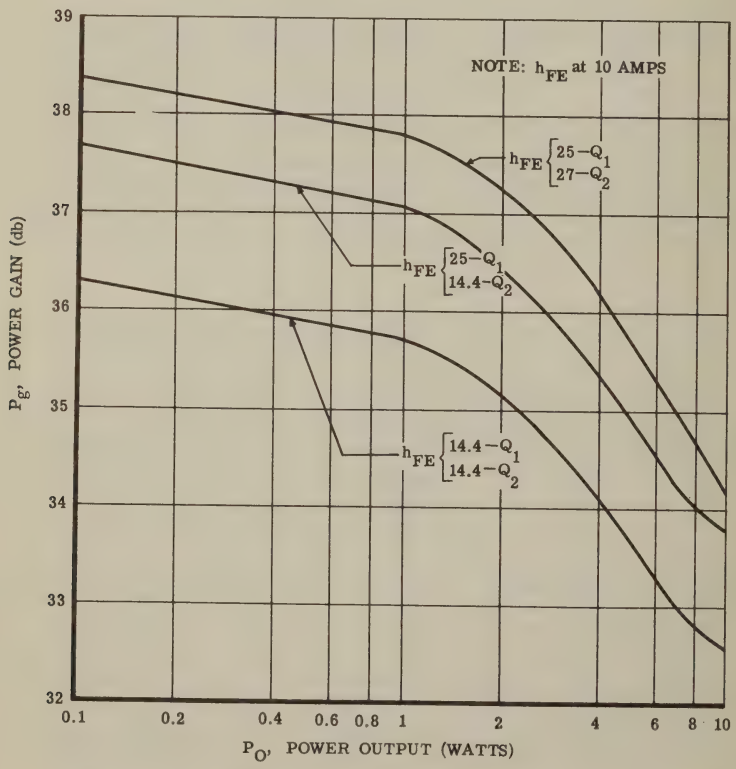


Figure 3-54 — Power Gain Versus Power Output (10 Watt Push-Pull)

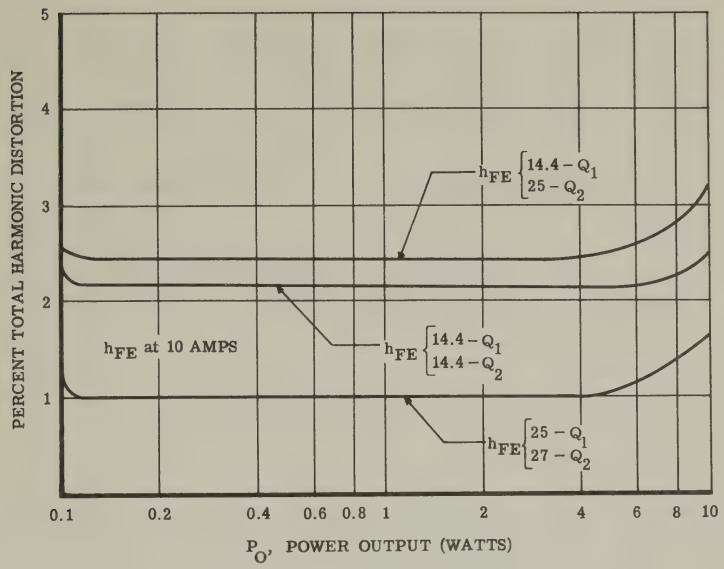


Figure 3-55 — Distortion Versus Power Output (10 Watt Push-Pull)

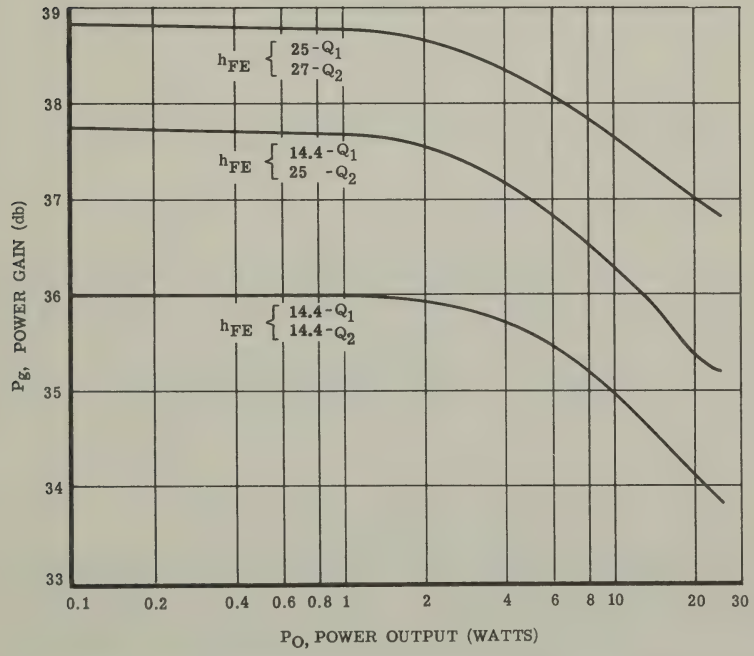


Figure 3-56 — Power Gain Versus Power Output (25 Watt Push-Pull)

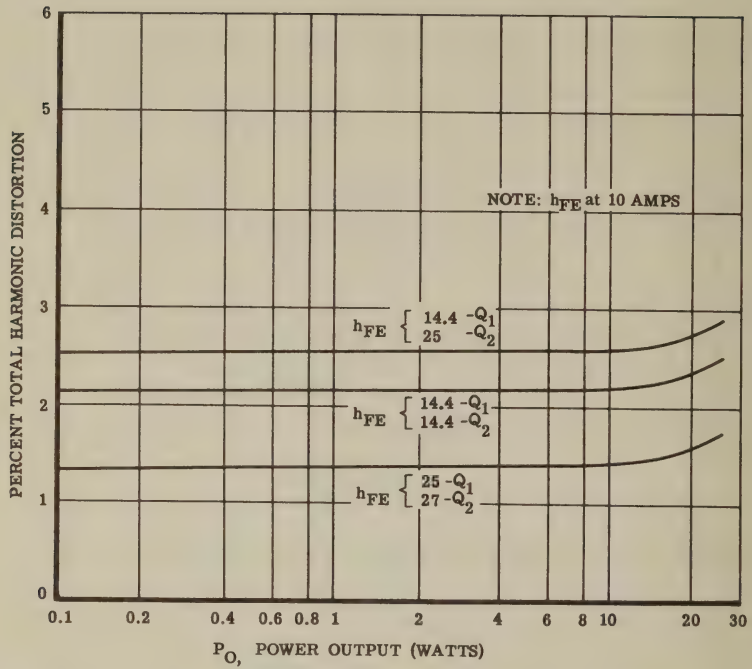


Figure 3-57 — Distortion Versus Power Output (25 Watt Push-Pull)

In comparing the 10-watt single-ended amplifier with the 10-watt push-pull amplifier, it can be noted that only at very high powers is the distortion lower for the push-pull stage. This is due to the difficult problems of matching transistors and minimizing crossover distortion. Logically then, for a low-power operation where efficiency is not important, one can effectively use a single-ended Class A stage. The Class B stage must be used when efficiency is important and it is always important at high powers where the problem is to provide sufficient heat sinks.

3-17 — A 2-Watt High-Fidelity Amplifier

INTRODUCTION: Class A stages are most satisfactory at low power levels. To produce an amplifier with a reasonable power gain and low signal input voltage requirements, the emitter-follower — common-emitter configuration shown in Figure 3-58 was chosen. It permits the power transistor to be driven from a low impedance source, which minimizes distortion and easily lends itself to direct coupling.

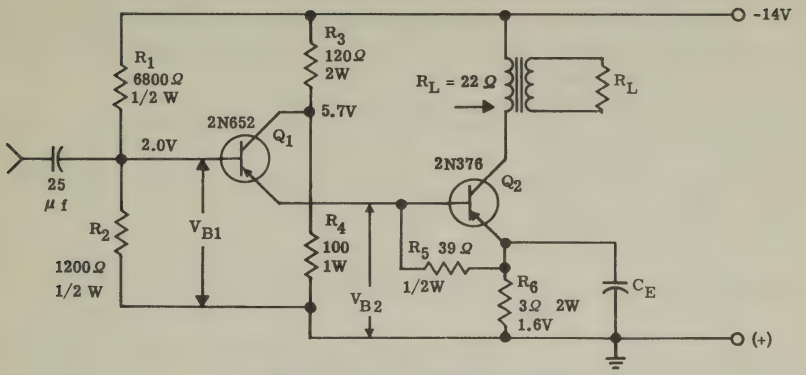


Figure 3-58 — 2 Watt Amplifier

CIRCUIT DESCRIPTION: R_1 and R_2 form the bias network for the entire amplifier. Their values will be determined by R_6, the required stabilization, and the desired value of quiescent current in Q_2. They should be chosen so that $V_{B1} = I_{Q2}R_6 + 0.4$ for germanium transistors. The 0.4 volt accounts for the sum of the drops across the base-emitter junctions. With proper design, I_{CBO} in Q_2 will have negligible effect upon quiescent point stability, but I_{CBO} in Q_1 is important. Thus, knowing the maximum expected I_{CBO} at maximum operating junction temperature, the permissible shift in V_{B1} for a given stability may be computed. Then the values of R_1 and R_2 are determined.

Since the emitter current of Q_1 equals the base current of Q_2 plus some additional drain through R_5, maximum values of Q_1 emitter current will occur when the lowest gain transistors are used for Q_2. Knowing this, R_3 and R_4 are chosen so that the minimum V_{CE} is about 1 volt under peak signal conditions. This will significantly increase the stability by operating Q_1 at the lowest possible voltage, resulting in less power dissipation and less I_{CBO}.

R_6 largely determines the stability of the system and is the sole determinant of the tolerable variation in current gain of Q_2. It should be chosen so that the voltage drop across it is large compared with the changes in base-to-emitter voltage required to keep emitter current constant over the expected temperature range for the various types of transistors proposed for Q_2. Generally, a 1.5-volt drop will ensure excellent stability when germanium transistors are used. R_5 serves to improve the circuit with regard to I_{CBO} in Q_2. The I_{CBO} of Q_2 will cause a few millivolts shift in V_{B2}. This causes little change in the collector current of Q_2 because of the stabilizing action of R_6; however, a drastic change in the collector current of Q_1 results. R_5 causes the current in Q_1 to be higher than that required to drive Q_2 to cutoff. Thus, some loss in current due to I_{CBO} in Q_2 will not limit the power output. R_5 will lower the input impedance of Q_2 and cause a loss of power gain through Q_2, but it can be shown that this is slight as long as R_5 is not smaller than the input resistance of Q_2. Over-all power gain will remain virtually unchanged, because normally the input impedance of Q_1 will be much greater than the shunt resistance of the bias network.

STABILITY: I_{CBO} can be simulated by using a high-voltage battery in series with a large resistance to produce the desired constant current. The results of I_{CBO} simulation are shown in Table 3-1. Power output and distortion were essentially unaffected by different value of I_{CBO}.

TABLE 3-1 — I_{CBO} STABILITY

Collector Current	$I_{CBO} = 0$	$I_{CBO} = 120\ \mu A$ in Q_1	$I_{CBO} = 2$ mA in Q_2	$I_{CBO} = 120\ \mu A$ in Q_1 and 2 mA in Q_2
I_{Q1} (mA)	10.6	11.3	7.7	8.5
I_{Q2} (mA)	510	550	520	560

Stability is adequate. Using Shea's stability definition $\left(S_I = \frac{\Delta I_E}{\Delta I_{CBO}}\right)$, S_I is about 5 for Q_1 and 4 for Q_2. The values of I_{CBO} are representative of actual values encountered when operating this amplifier at an ambient temperature of 60°C. I_{CBO}, however, is not the only undesirable result of high-temperature operation. The forward voltage drop of the emitter-base junction decreases, causing additional emitter current. Figure 3-59 illustrates the results of this effect. Motorola 2N652 and 2N376 transistors were used in the circuit. Temperatures shown are ambient temperatures. The power transistor junction temperature was approximately 25°C higher because of the heat dissipator which was used. The junction of Q_1 was only about 10°C higher, since the can was fastened to the chassis by a fuse clip. Performance over the temperature range of −25°C to +60°C is adequate.

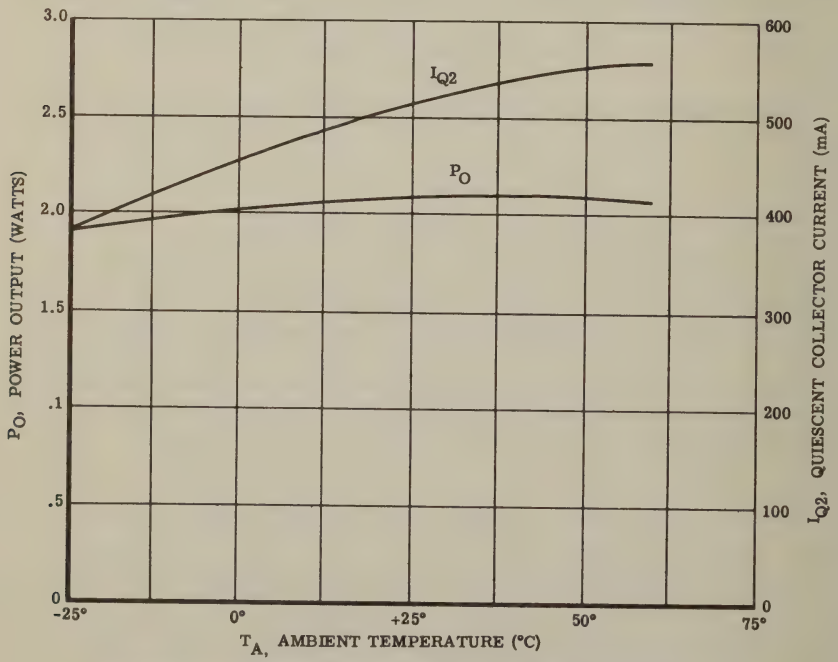


Figure 3-59 — Power Output and Q_2 Collector Current Versus Ambient Temperature (2 Watt Amplifier)

Excessive I_{CBO} in Q_2 will reduce the current through Q_1 to a value insufficient to provide full drive. To help determine the optimum value of R_5, Figure 3-60 was prepared using I_{CBO} simulation. The figure shows the expected current through Q_1 and the effect of I_{CBO} on power output when various values of R_5 are used. In actual use, of course, some compensation would occur at high temperatures, because I_{CBO} in Q_1 and changes in the base-emitter conductance of

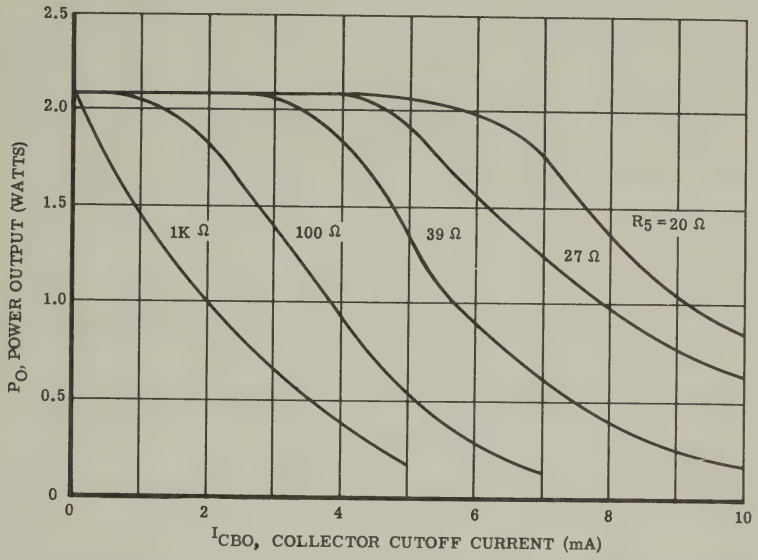


Figure 3-60 — Power Output Versus R_5 and I_{CBO} of Q_2 (2 Watt Amplifier)

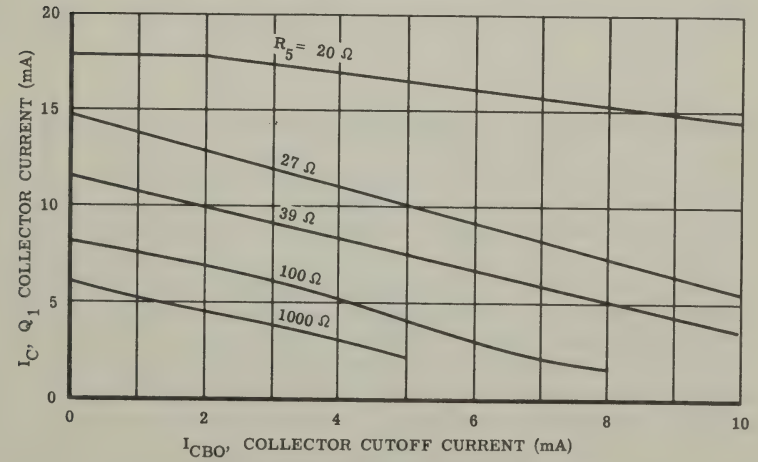


Figure 3-61 — Collector Current of Q_1 Versus R_5 and I_{CBO} of Q_2

the transistors would increase the current through Q_1. Other characteristics of the amplifier are virtually unchanged, as R_5 is varied over the range shown. With the circuit in Figure 3-58, I_{CBO} should not exceed 3.0 mA at 12 volts V_{CE} and at the highest junction temperature. As the data shows, when $R_5 = 20$ ohms, I_{CBO} could reach 7.0 mA with no adverse effects. However, lower I_{CBO} in the power transistor permits a sizeable reduction in the dissipation required of Q_1. The effect of R_5 on the current through Q_1 is shown in Figure 3-61.

Several transistors having a wide range of current gain were used in both stages of Figure 3-58. The current gain of the driver need only be over 75 to have no measurable effect upon performance; therefore, type 2N652 was chosen. Figure 3-62 shows the effect of the D-C current gain of Q_2 upon the collector currents of both transistors. From this curve, it appears that a minimum of 60 is required. Several Motorola types were used for the power transistor. Type 2N376 has a reasonable design center and is used in all the data which follows.

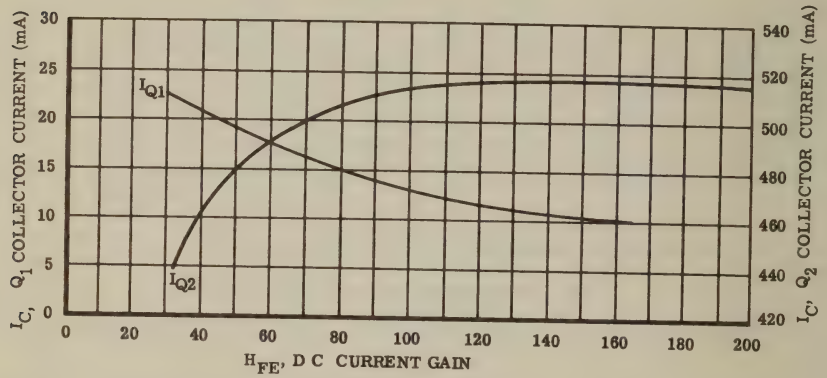


Figure 3-62 — Collector Currents of Q_1 and Q_2 Versus DC Current Gain (2 Watt Amplifier)

FREQUENCY RESPONSE AND DISTORTION: Harmonic distortion is shown in Figure 3-63. Values shown are typical. The frequency response at a low reference level is shown in Figure 3-64. The effect of bypassing, or rather attempting to bypass, the emitter of the output stage is shown by the lower curve. The bandwidth becomes too narrow and even a 4000-μf capacitor is not large enough for adequate low-frequency response. About 18 db more gain results and distortion is increased by about a factor of six. Signal source impedance for these measurements was 10,000 ohms. Response improves and distortion increases slightly as the source impedance is lowered. Distortion of the generator used measured 0.1%. The most significant performance curve is shown in Figure 3-65, which illustrates the power output at a constant total harmonic distortion of 1%. The half-power point is reached at 10 kc.

The output impedance looking back from the transformer primary is approximately 310 ohms. Therefore, to provide damping, a feedback voltage taken from the output transformer should be applied to the stage preceding the driver.

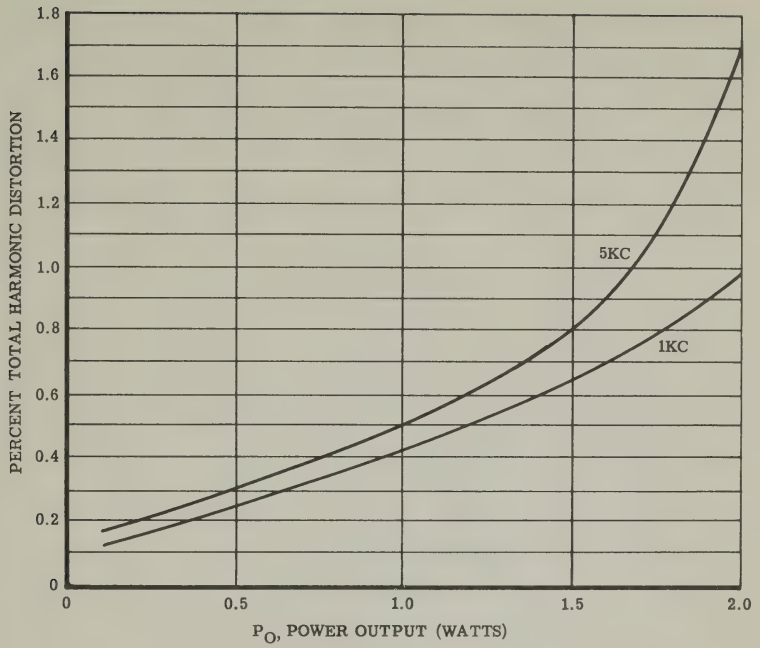


Figure 3-63 — Distortion Versus Power Output (2 Watt Amplifier)

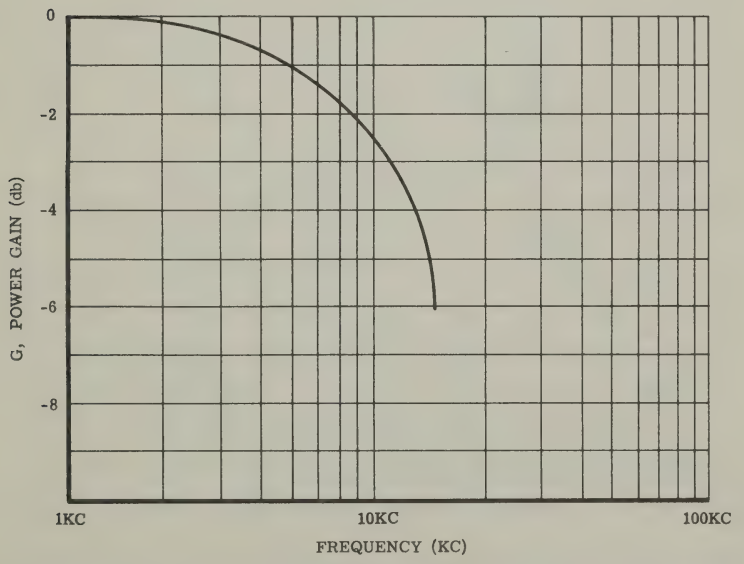


Figure 3-64 — Typical Power Gain Versus Frequency (2 Watt Amplifier)

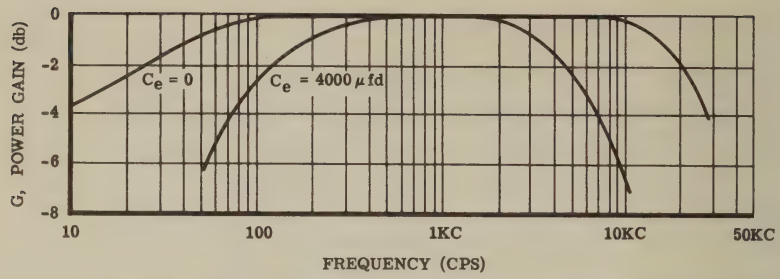


Figure 3-65 — Effect of Bypass Cacapitor on Frequency Response at Constant 1% Distortion (2 Watt Amplifier)

CIRCUIT VARIATIONS: To increase the gain of the system transformer coupling into the input could be used. By matching to the high input impedance of Q_1, which is approximately 15,000 ohms, an additional 12 db of gain could be realized. However, gain will vary with transistor parameters and distortion will be a function of the source resistance. Stability with regard to I_{CBO} in Q_1 could be improved because with transformer coupling the bias resistors, R_1 and R_2, can be made very small, since they no longer shunt the input. Figure 3-66A shows how stability can be improved in this manner.

Another method of reducing the shunt effect of R_1 and R_2 to increase the gain is to utilize the resistance multiplying circuit for Q_1, as shown in Figure 3-66B. The feedback voltage must be taken from the emitter of Q_2, however, because Q_1 will not tolerate any additional loading. This system will provide about 6 db more gain at the expense of 50% more distortion and some variation of power gain with transistor parameters. If the signal source has a high impedance, this approach may have merit.

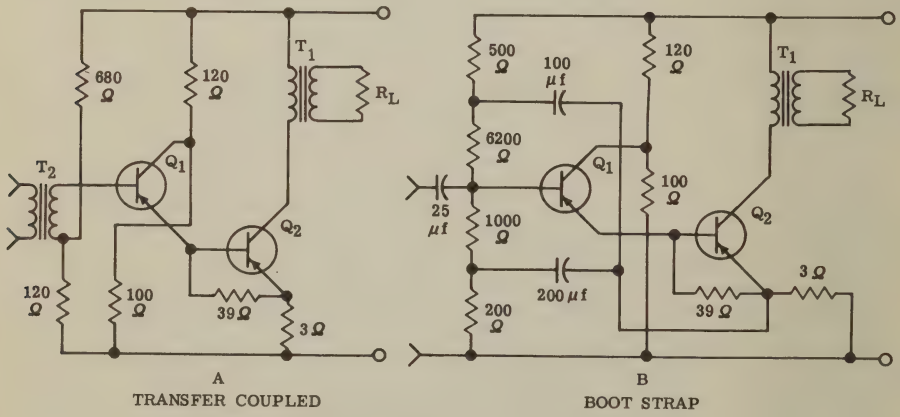


Figure 3-66 — Modified 2 Watt Amplifier

3-18 — A 10-Watt High-Fidelity Amplifier

Selection of an output stage for an amplifier should take into account the following:

1. Distortion
2. Power Gain
3. Output Impedance
4. Effects of Mismatching
5. D-C Stability

DISTORTION: The transfer characteristics of the three configurations — common emitter, common base, and common collector (emitter follower) — are shown in Figures 3-67, 3-68, and 3-69. The curves show the effects of voltage drive, Rg = 0, and current drive, where Rg is much larger than the input impedance of the transistor. Any practical source impedance would produce a curve intermediate to the curves shown. Note the rather poor linearity of the common-emitter stage, regardless of the source impedance used. However, as has been mentioned earlier, emitter resistance and a low impedance source will improve this condition greatly. The common-base circuit has excellent current linearity as one would expect, since α is nearly always close to unity. However, a low source impedance, which one might be tempted to use in order to match the driving stage to the input, would result in considerable distortion.

The common-collector stage exhibits the same nonlinearity with current drive as does the common emitter. This is due to the loss in current gain at high collector currents. However, with voltage drive the common-collector stage is remarkably linear. This is because the base-to-common and emitter-to-common voltages can differ only by the drop across the base-emitter junction, which changes very little with collector current. Note the lack of offset voltage in any configuration when current drive is used. Thus, for a low distortion Class B stage, a current driven common-base configuration should be used since no offset bias is required. A voltage driven common-collector stage could also be used, but a small bias voltage would be required.

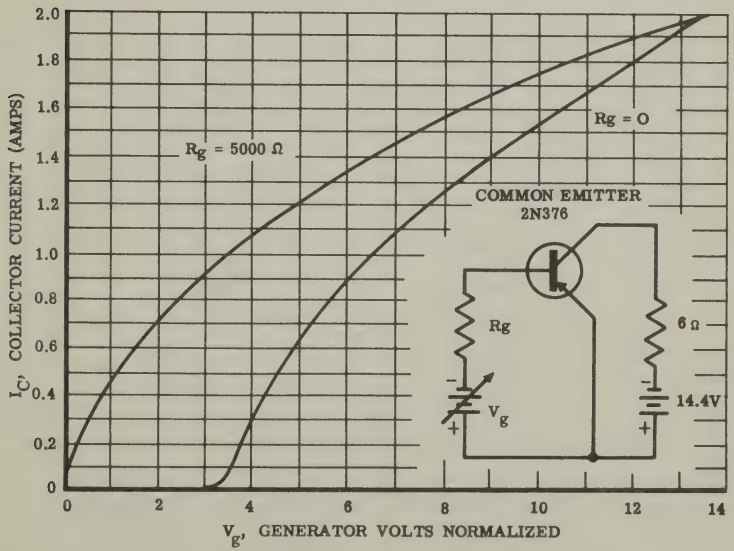


Figure 3-67 — Common-Emitter Transfer Curve

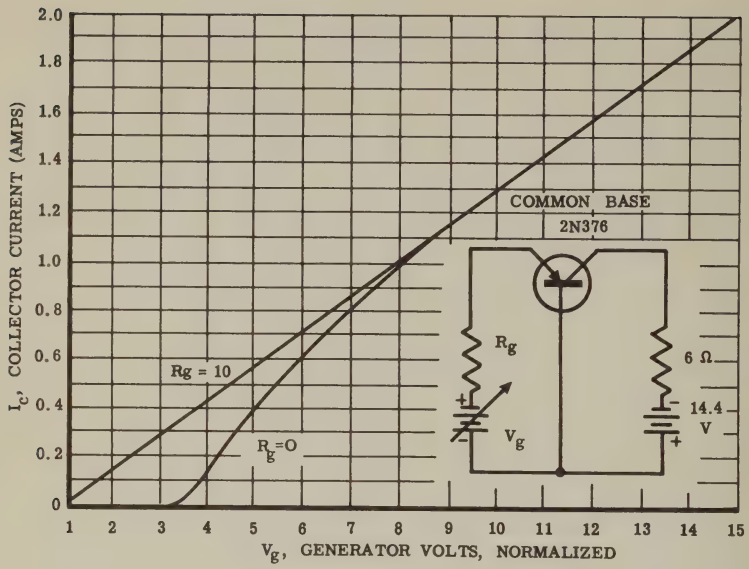


Figure 3-68 — Common Base Transfer Curve

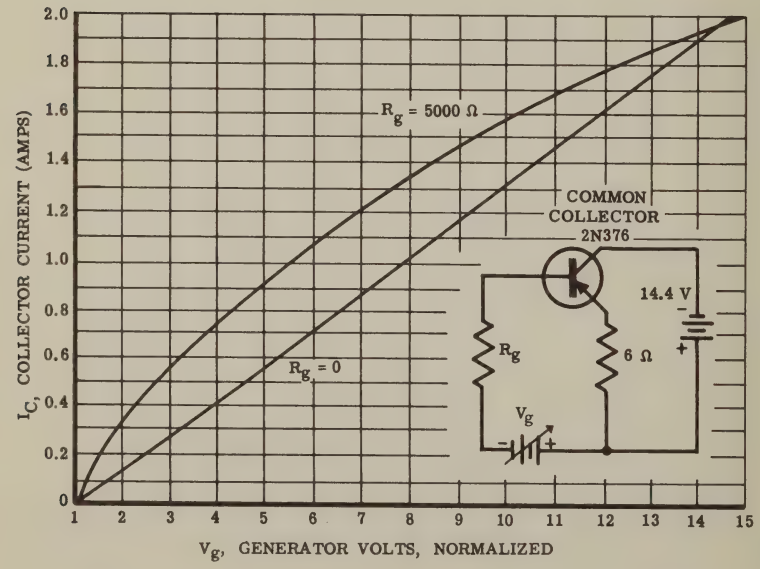


Figure 3-69 — Common Collector Transfer Curve

POWER GAIN: The common-emitter stage provides a power gain which is the highest of the three configurations — approximately equal to current gain times voltage gain.

The common-base stage has a power gain equal to the common-emitter voltage gain. However, with the low load resistance needed for a 10-watt amplifier from a 12-volt source and the high source impedance required for good linearity, the gain would be too low to be useful.

The common-collector stage may be thought of as a common-emitter stage with 100% voltage feedback. Thus only a current gain of h_{FE} results, but this could be adequate.

OUTPUT IMPEDANCE: To provide damping, the speaker should be driven from a low impedance source. This could be provided by a feedback voltage taken from the speaker and applied to any stage in the amplifier. However the current gain cutoff frequency of ordinary power transistors operated common emitter is in the 5 to 10 kc region. The associated phase shift in the audio passband makes multistage feedback difficult. Even one stage and a transformer could oscillate. Therefore, the simplest single-stage feedback circuit, the common-collector amplifier, is usually recommended.

EFFECT OF MISMATCHING: Since in Class B stage, each transistor operates for only one-half cycle, each side of a push-pull pair should have identical gain. The degree of unbalance will be evident as high even-harmonic distortion. A nonlinear transfer characteristic for a side will appear as odd-harmonic distortion.

With a current driven common-base pair, obtainining a balance is no problem since current gain is very near unity.

Distortion as a function of current gain mismatch ratio for the common-emitter and common-collector configuration is shown in Figures 3-70 and 3-71. A maximum ratio of 2:1 is shown as manufacturers often use this ratio as a production tolerance for h_{FE}. Optimum bias current was used for each amplifier. Driver impedance was optimized at 20 ohms base-to-base for the common emitter. 60 ohms base-to-base was judged to be a practical lower limit for the common-collector amplifier.

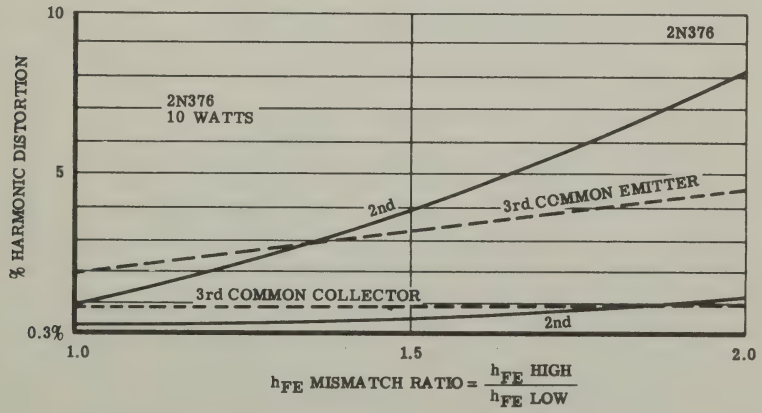


Figure 3-70 — Effect of h_{fe} Mismatch on 10 Watt Distortion

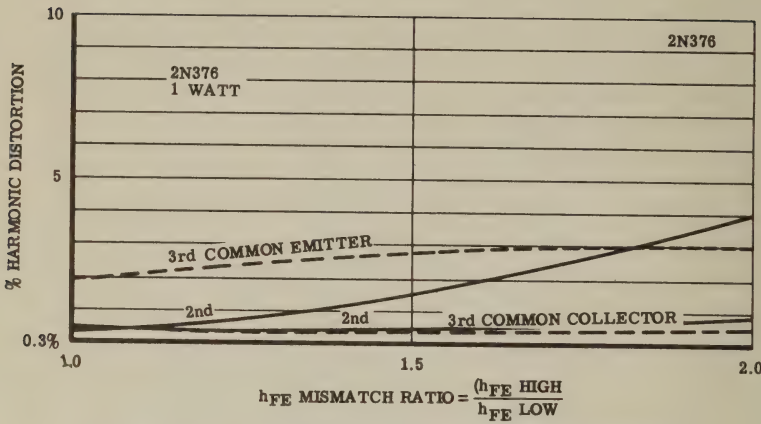


Figure 3-71 — Effect of h_{fe} Mismatch on 1 Watt Distortion

As Figure 3-71 shows, third-harmonic distortion in a common-emitter stage is too high to be useful in a nonfeedback amplifier. The second-harmonic distortion is acceptable only with very careful balancing. The common-collector stage however, exhibits less than half the third-harmonic distortion of the common emitter; second harmonic is very low. Neither component is affected much by mismatch. This is understandable, since the transconductance of an emitter-follower is nearly equal to $1/R_L$, therefore transistor parameters are not too important.

A particularly frustrating aspect of common-emitter operation is evidenced in Figure 3-71 which shows that distortion is high, even at the one-watt level. Common collector distortion is nearly that of the generator, 0.3%.

D-C STABILITY: The common-base circuit is the most stable, with common-collector and common-emitter stages following in order.

OUTPUT STAGE: The common-collector stage was chosen for this amplifier for the following reasons:

1. Low distortion
2. Reasonable power gain
3. Low output impedance
4. Non-critical matching
5. Reasonable stability.

COMPLETE AMPLIFIER: The circuit of the complete amplifier is shown in Figure 3-72. A power supply for operation from an A-C line is shown. The supply exhibits excellent regulation and low ripple which is an important requirement when Class B amplifiers are used.

Since the common collector output stage requires a low impedance driving source, a common collector driver stage is used. Transformer coupling is used since it provides excellent D-C stability, and permits reserve driving voltage to be obtained. The D-C winding resistance of the output transformer is used as an emitter resistor to stabilize the output stage. The driver operates push-pull

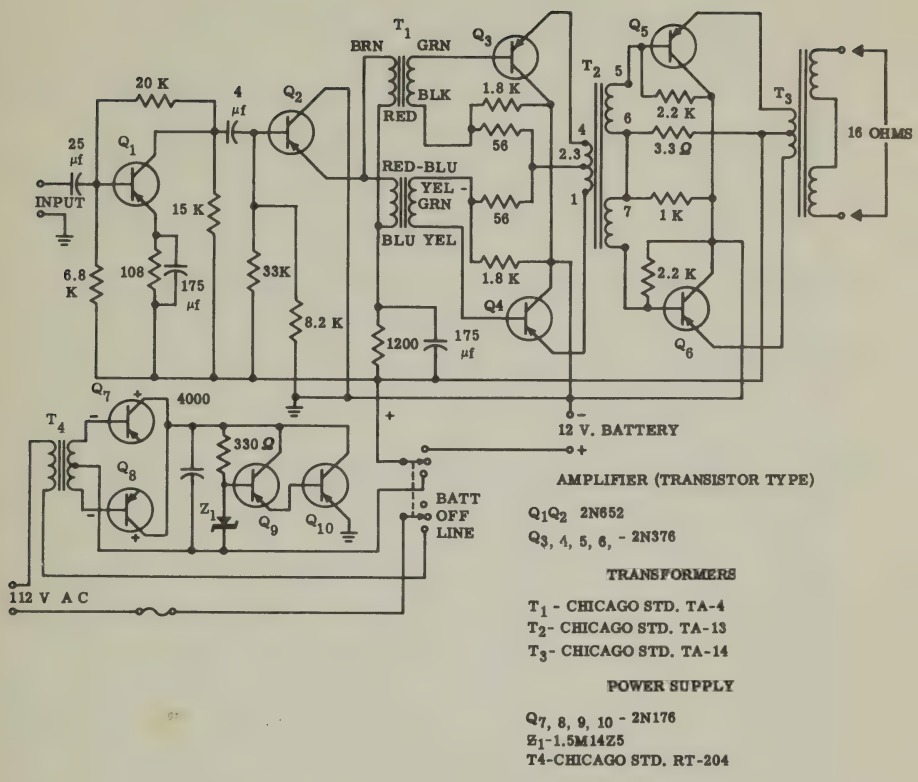


Figure 3-72 — 10 Watt Hi-Fi Amplifier

Class A for low distortion and to eliminate direct current saturation effects in the transformer, thus reducing the size and cost of this component. Since the driver also must be driven from a low impedance source, another common-collector stage is used. It is also transformer coupled to provide voltage step-up and phase inversion for the push-pull drivers. The first stage is a voltage amplifier.

Frequency response is shown in Figure 3-73 and harmonic distortion in Figure 3-74. Intermodulation distortion at 10 watts output is 2.9%, measured by the SMPTE Method, using frequencies of 60 and 6000 cps mixed 4:1.

The D-C current drain is 180 mA, with no signal supplied. Most of this is drawn by the push-pull driver. Total drain increases to 1.3 amperes under full output power.

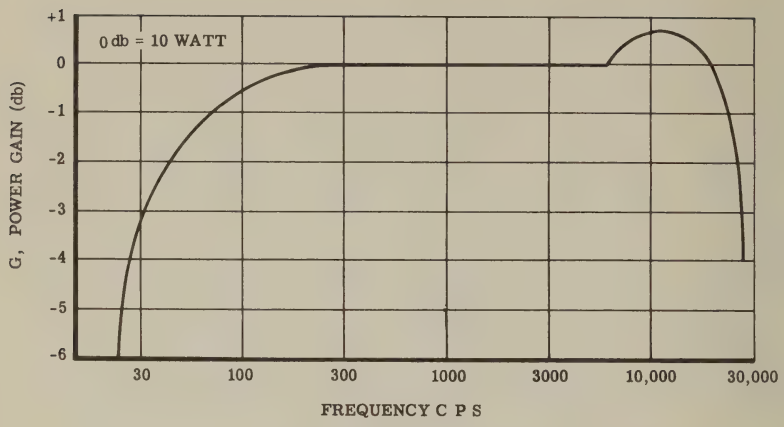


Figure 3-73 — Frequency Response (10 Watt Hi-Fi Amplifier)

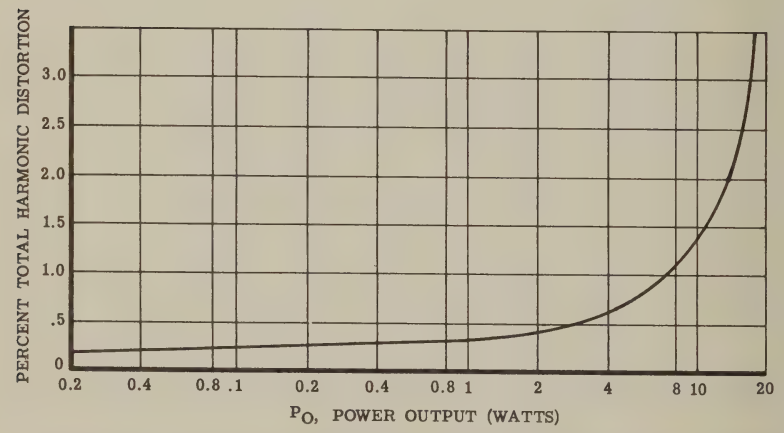


Figure 3-74 — Distortion Versus Power Output (10 Watt Hi-Fi Amplifier)

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1. Fewer, D. R., "Design Principles for Junction Transistor Audio Power Amplifiers," IRE Transactions and Audio, Vol. AV-3, No. 6, Nov.-Dec. 1955, page 183.
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CHAPTER IV

Power Transistor Switching Applications

4-1 — Switching Characteristics

One of the early applications of the power transistor was as a switching device for D-C to A-C conversion in vehicle radio power supplies. In this application the transistor electrically performs the same function as the mechanical vibrator which it replaced, changing the constant D-C voltage into a square-wave or sine-wave voltage.

Schematically the switching action of a transistor switch is simulated in Figure 4-1 which shows a switch opening and closing to alternately permit current through an output resistance. As the switch is closed, the entire battery potential is applied suddenly to the output resistance and the current increases to its maximum value of $\frac{V_R}{R_L}$. When the switch is opened, the voltage across the output resistance drops to zero, causing the current flow to drop also. At this time the entire battery voltage is across the switch. The waveform showing voltage buildup is indicated in Figure 4-2.

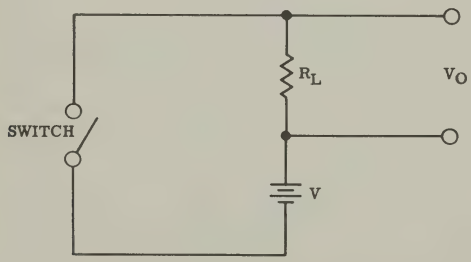


Figure 4-1 — Basic Switch Circuit

It will be noted that the output pulse does not duplicate the input pulse exactly. Even though the input is a step function, there is a finite time required for the switching action (on-off or off-on) to take place. The term "rise time" has been defined as the time required for the current to rise from 10% to 90% of the total current rise.

Switching action can be obtained by using a transistor in place of the mechanical switch (Figure 4-3). The transistor is driven on and off by applying a square wave across the base-emitter junction, thereby alternately forward biasing and reverse biasing the junction. The transistor amplifies a voltage (or current) when the emitter-base junction is forward biased and the collector-base junction is reverse biased. When both junctions are reverse biased, no transistor action takes place and only leakage currents are present.

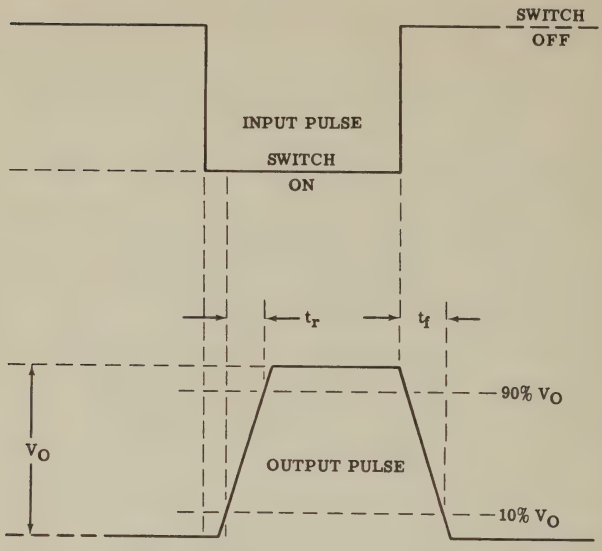


Figure 4-2 — Input and Output Waveforms of Basic Switch

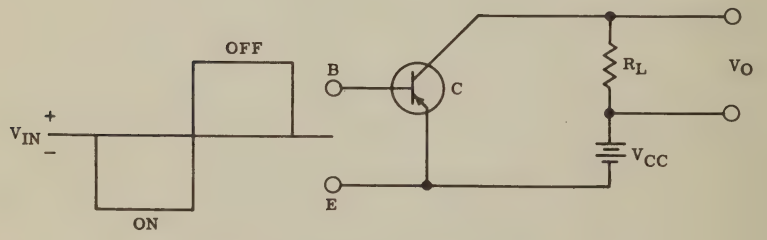


Figure 4-3 — Basic Transistor Switch

Consider the situation in which the transistor is thought of as a perfect switch and is a complete open circuit when fully off and a complete short circuit when fully on. Under these ideal conditions, the current will be limited by the ratio of collector voltage divided by load resistance, $\frac{V_{CC}}{R_L}$ (see Point A, Figure 4-4). This point represents the full "on" situation. When the transistor is open, there will be zero current flow and the entire battery voltage (V_{CC}) will be across the collector-emitter terminals. This "off" condition is represented on the output characteristic as Point D.

However, from a practical viewpoint we cannot completely open the transistor because in the "off" condition leakage current, I_{CBO}, continues to flow. This actual condition is represented by Point C on the output characteristic curve. Neither can we completely short circuit the device since the "on" current

is limited by the intersection (Point B) of the saturation resistance and the load line. These conditions may be represented by the following equations:

$$I_{on} = \frac{V_{CC} - V_{CS}}{R_L}, \text{ and} \tag{4-1}$$

$$I_{off} = I_{CBO}. \tag{4-2}$$

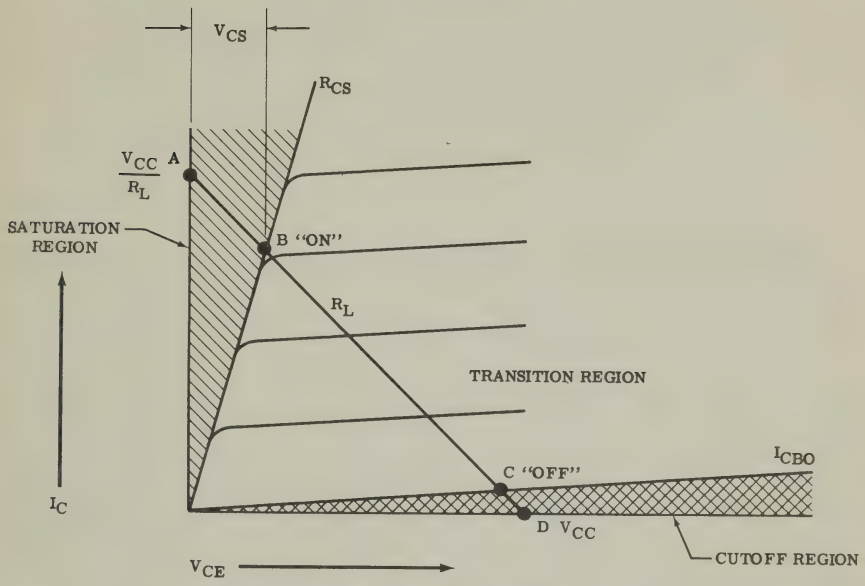


Figure 4-4 — Transistor Output Switching Regions

When the base drive is sufficient to cause the maximum "on" condition, the switching mode is called saturated operation. If the on drive is not sufficient to saturate, the switching mode is called nonsaturated operation. In either mode the transistor is being switched from on to off and off to on through the transition region of the transistor output characteristics. The speed of this switching is limited by the rise and fall times of the device. In addition, during saturated operation the transistor will not respond immediately to being turned off when the base drive is reversed since a delay time exists to allow the operating point of the transistor to leave the saturation region. This delay time is called storage time. The wave shapes associated with transistor switching are illustrated in Figure 4-5.

It is common practice to refer to the on base current as I_{B1} and the off base current as I_{B2}. The rise, t_r, fall, t_f, and storage, t_s, times are indicated on the waveshapes. In addition, there is the time required for the current to rise to 10% of the maximum value — called delay time, t_d.

In following sections we will show some of the response characteristics of power transistors. The power loss due to switching will be explained in terms of transistor characteristics. Also specific switching circuits, such as TV sweep and D-C to A-C inverters, will be described.

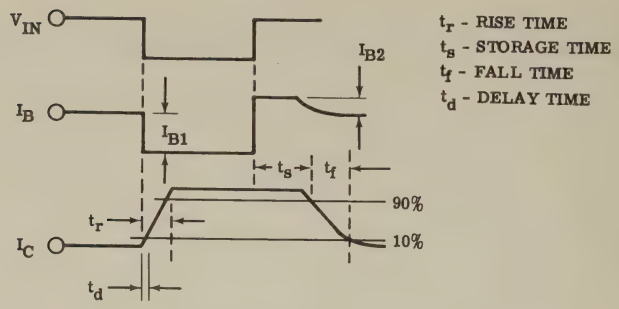


Figure 4-5 — Input and Output Wave Shapes

SATURATED OPERATION: A transistor is said to be in saturation when both junctions are forward biased. When operated in the saturated region, where $I_C = \frac{V_{CC} - V_{CS}}{R_L}$, rise time varies inversely with the common-base current gain frequency cutoff, $f_{\alpha b}$, and, for a constant collector current, with the on base current, I_{B1}. It also varies directly with collector current when the base current is held constant.

Storage time is a direct function of forward base drive current, I_{B1}, and common-emitter current gain, h_{FE}, and an inverse function of $f_{\alpha b}$ and reverse base current, I_{B2}. Storage time is the interval required to remove the excess minority carriers near the collector-base junction when the transistor is operating under saturated conditions. I_{B2} is actually the current attributable to these minority carriers as they are being swept clear of the collector-base junction, and their presence accounts for collector current flowing after termination of the input pulse. The lower the saturation voltage, the greater the storage time. Fall time is a direct function of collector current and an inverse function of $f_{\alpha b}$ and I_{B2}.

NONSATURATED OPERATION: Storage and fall time can be reduced considerably by not allowing the transistor to saturate during forward conduction, although this is done at the expense of rise time. When operating under the nonsaturated condition the collector current, when turned on by an input pulse, rises on an exponential curve (with respect to time) to a value of $h_{FE}I_{B1}$. There is no accumulation of minority carriers in the base-collector region, so storage time is not present and fall time is reduced 15 to 40% for a given collector current. Figure 4-6 shows the difference in the output pulse when a typical transistor is pulsed into saturation, and when the collector-emitter voltage is held to a minimum of 4 volts to assure a nonsaturated condition.

In nonsaturated operation, fall time varies inversely with frequency cutoff. Nonsaturated rise and fall times t_r and t_f are related to $f_{\alpha e}$ according to the following empirical relations:

$$t_r \times f_{\alpha e} = 0.3$$
$$t_f \times f_{\alpha e} = 0.6$$

where

t_r = nonsaturated rise time between the 10% to 90% points in microseconds,

t_f = nonsaturated fall time between the 10% to 90% points in microseconds, and

$f_{\alpha e}$ = common emitter cutoff frequency, cps.

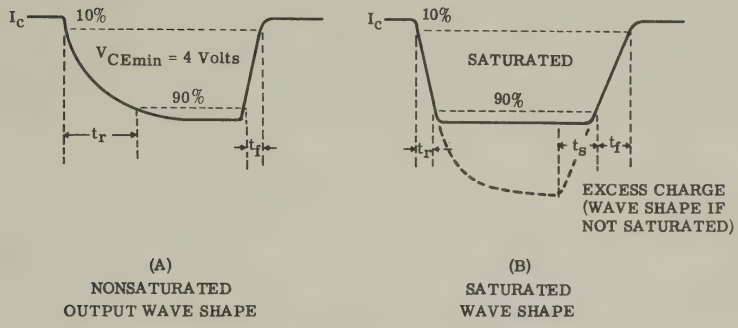


Figure 4-6 — Typical Wave Shapes

SPEED-UP CAPACITOR: When it is impractical to use a back bias to increase I_{B2} and reduce storage and fall time, a capacitor can be inserted across the base-current limiting resistor to reduce all switching time (Figure 4-7). An optimum value exists for the bypass capacitor (C_1) depending on the transistor and the amount of base current. Generally the current limiting resistor (R_1) is set so that:

$$I_B = \frac{2I_C}{h_{FE\ min}}. \tag{4-3}$$

$$\text{Thus, } R_1 = \frac{(V_{IN} - V_{EB\ max})\ h_{FE\ min}}{2I_C}, \text{ or} \tag{4-4}$$

$$R_1 = \frac{V_{IN}\ h_{FE\ min}}{2I_C} - \frac{h_{FE\ min}}{2g_{FE\ min}}. \tag{4-5}$$

The value of C_1 is then found experimentally to minimize t_s and t_f. For example, a Motorola 2N627 power transistor when switching $I_C = 10$ amps and $V_{IN} = 10V$ requires a 0.5 μf bypass capacitor. Values from 0.1 μf to 5 μf have been noted for different transistors, and input voltage levels.

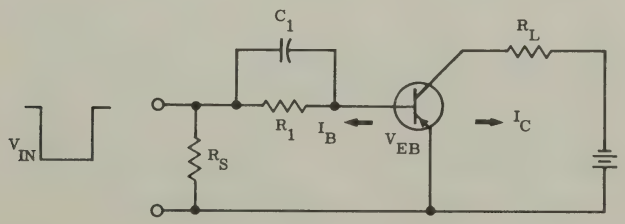


Figure 4-7 — Speed-Up Capacitor

4-2 — Switching Characteristics of Motorola Power Transistors

The rise, fall, and storage times as functions of collector current and forward and reverse base current have been evaluated for Motorola 10- and 25-ampere power transistors, types 2N627 and 2N1163. Figure 4-8 shows the circuit used to obtain the data. Both saturated and nonsaturated operation was tested.

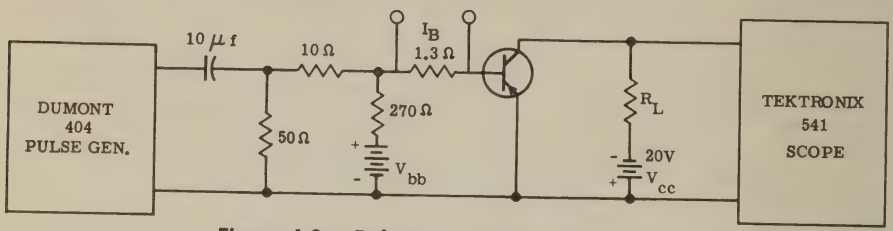


Figure 4-8 — Pulse Response Test Circuit

The saturated rise time as a function of I_{B1} and collector current is shown in Figure 4-9. Figure 4-9A applies to the 2N627 and Figure 4-9B to the 2N1163. An interesting point revealed by these curves is that with a forced gain $\left(B = \frac{I_C}{I_{B1}}\right)$ of 10 the rise time is almost independent of collector current. Other forced gain ratios tend to show similar effects. Another facet of saturated operation is that rise time will decrease as forced gain increases.

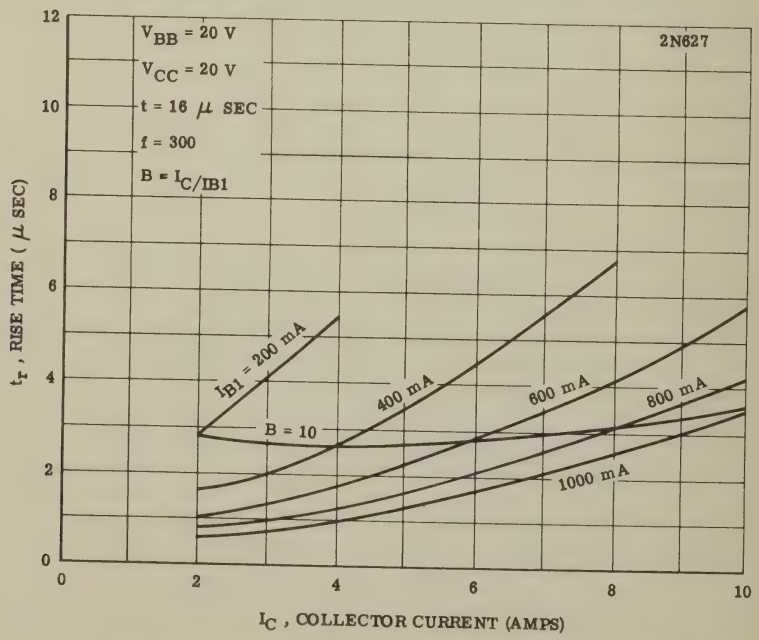


Figure 4-9A — 2N627 Saturated Rise Time Versus I_B and I_C

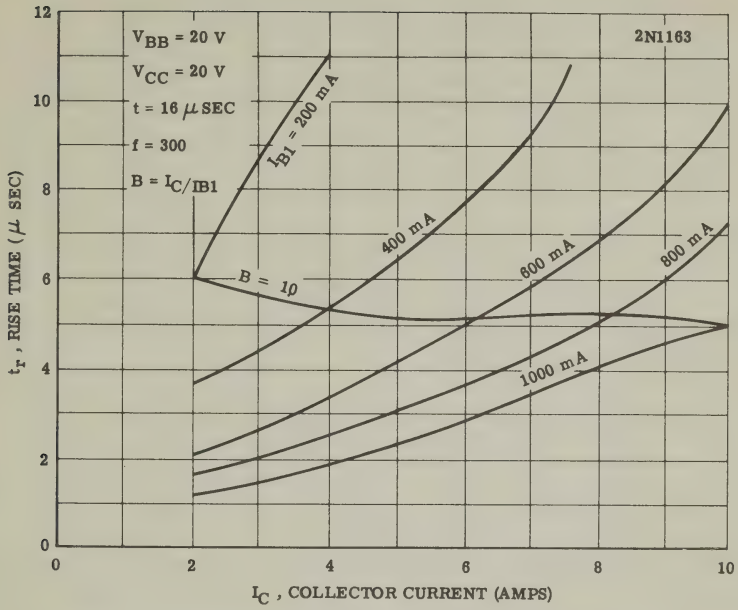


Figure 4-9B — 2N1163 Saturated Rise Time Versus I_B and I_C

The storage time in the saturated condition is affected by the on drive, the off drive, and the forced gain ratio. The storage time, as shown in Figures 4-10 and 4-11, decreases as forced gain increases and will go to zero as the forced gain approaches normal current gain h_{FE}, which is the nonsaturated case. Increasing the off drive I_{B2} will decrease the storage time.

The effects of circuit conditions on fall time can be observed from Figure 4-12. For similar reverse forced gain $\left(B_R = \frac{I_C}{I_{B2}}\right)$, the fall time is similar. As the reverse forced gain is decreased (that is, I_{B2} increased), the saturated fall time will decrease.

For nonsaturated operation we are concerned only with rise and fall time since storage time is not present. Figure 4-13 is an indication of the rise time as a function of collector current. There is no forced gain present and the rise time for the 2N627 decreases as collector-current increases whereas the reverse is true for the 2N1163. The fall time has been plotted as a function of base current, the collector current starting at 2 amperes and the base drive increased until 10 amperes were reached. As the base drive and hence collector current increased, the fall time increased for both the 2N627 and the 2N1163 as illustrated in Figure 4-14.

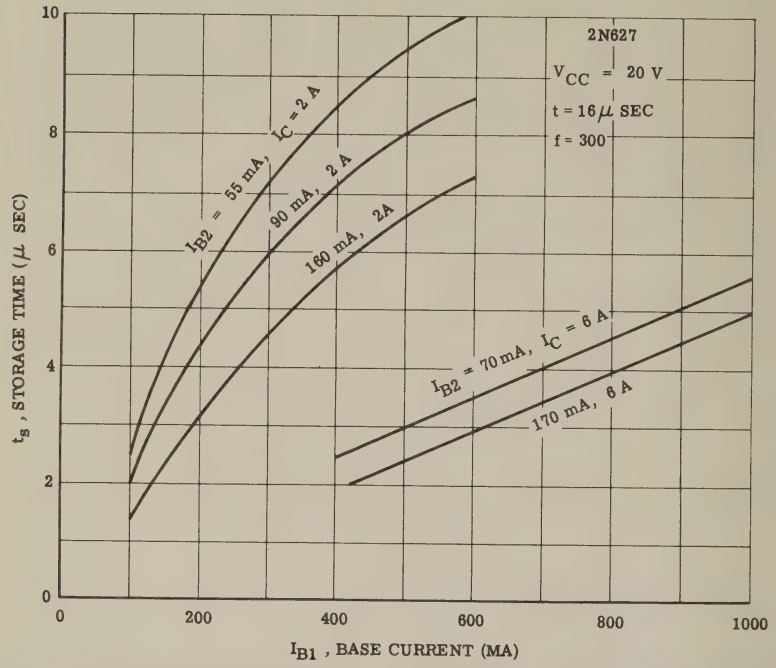


Figure 4-10 — 2N627 Saturated Storage Time Versus I_{B2} and I_{B1} at I_C = 2A and 6A

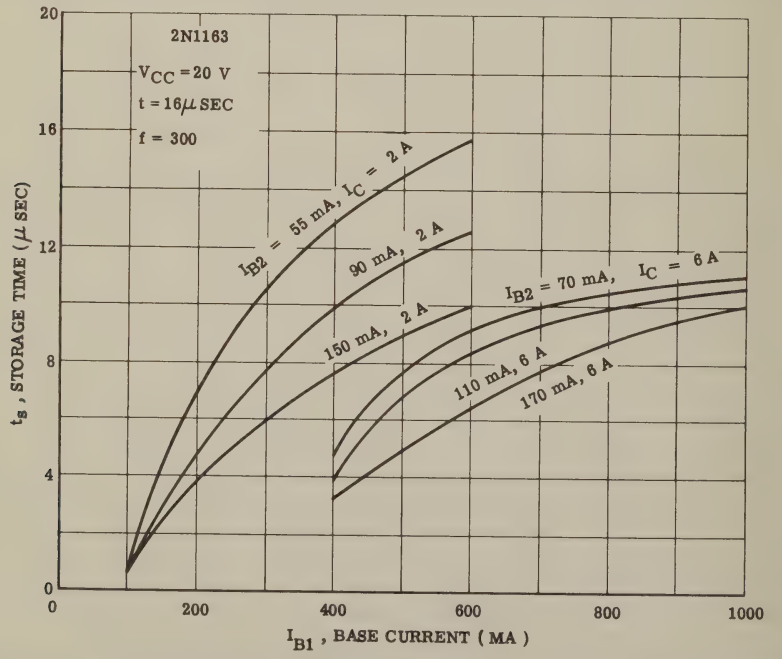


Figure 4-11 — 2N1163 Saturated Storage Time Versus I_{B2} and I_{B1} at I_C = 2A and 6A

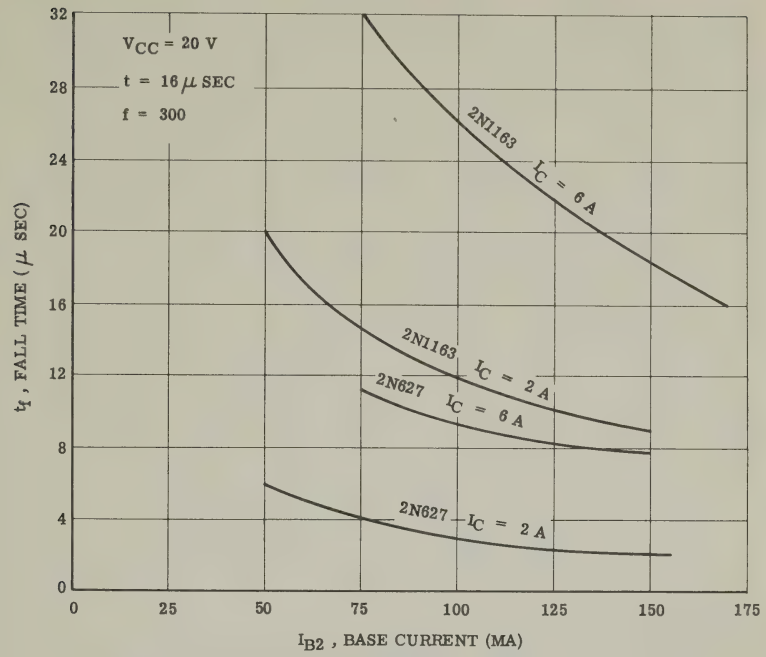


Figure 4-12 — Saturated Fall Time Versus I_{B2} at I_C = 2A and 6A

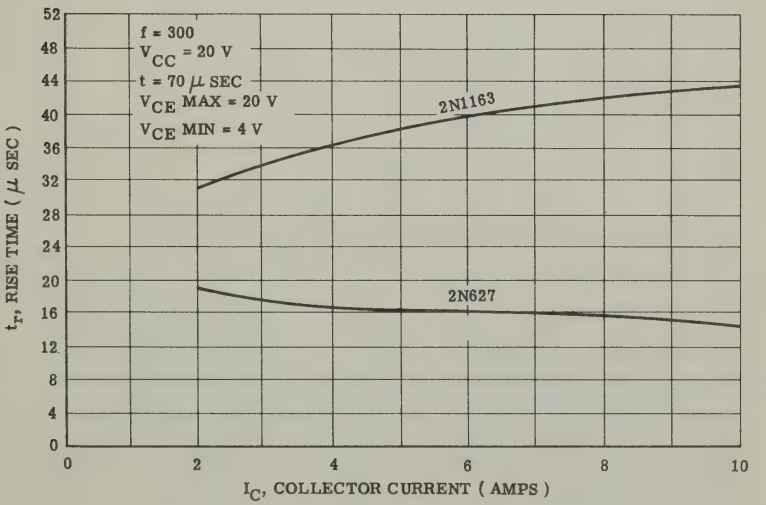


Figure 4-13 — Nonsaturated Rise Time Versus Collector Current

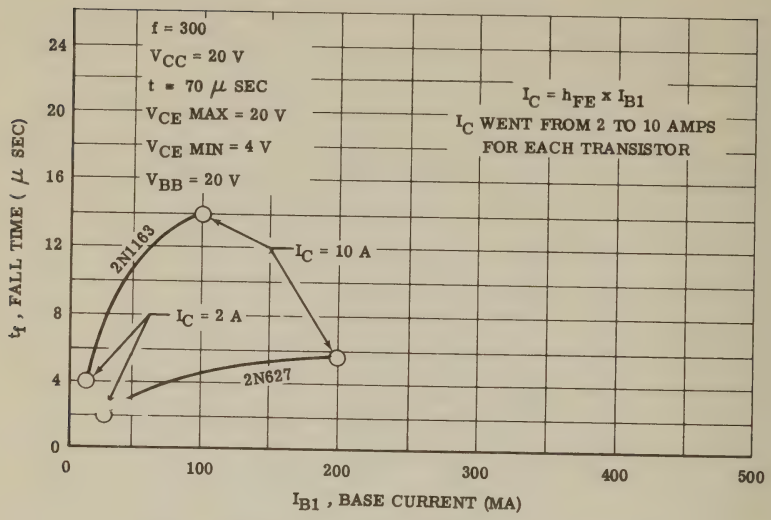


Figure 4-14 — Nonsaturated Fall Time Versus I_{B1}

4-3 — Switching Losses

Power losses in a converter are mainly the result of (1) the input power used during the on time, (2) the output power dissipation during on time, and (3) the switching power consumed going from on to off and from off to on.

On switching power loss may be calculated using the following equation ignoring "off" loss:

$$P_{Loss} = \frac{I_P}{6T}(2t_S V_P + 3V_{CS}T) \qquad (4\text{-}6)$$

where I_P is peak collector current,

V_P is peak collector voltage,

V_{CS} is minimum collector voltage,

T is the period of one cycle, (in seconds), and

t_S the switching time, (in seconds), $t_s = t_r = t_f$.

A derivation of the power loss equation (4-6) as used in switching modes follows. It is assumed the rise and fall times are the same, resulting in symmetrical switching times. Perfect wave shapes of collector voltage, current, and power for D-C to D-C converters are shown in Figure 4-15. The effect of frequency upon average power dissipation is shown in Figure 4-16.

Average power is, in effect, the sum of the energy dissipated during each part of the cycle divided by the total period.

$$P_{ave} = \frac{\sum_{o}^{T} P_f \Big]_{o}^{t_f} + P_{off} \Big]_{t_f}^{T/2} + P_r \Big]_{T/2}^{T/2 + t_r} + P_{on} \Big]_{T/2 + t_r}^{T}}{T}$$

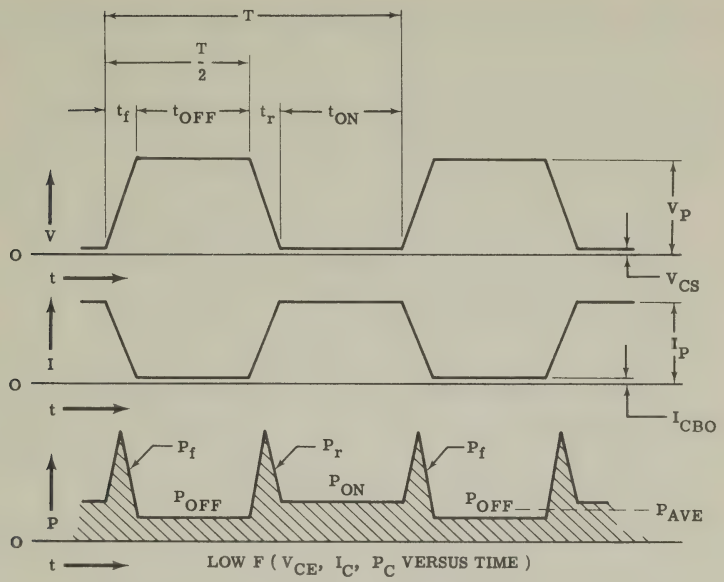


Figure 4-15 — Typical Wave Shapes of I_C, V_C, and P_C for D-C to A-C Inverters

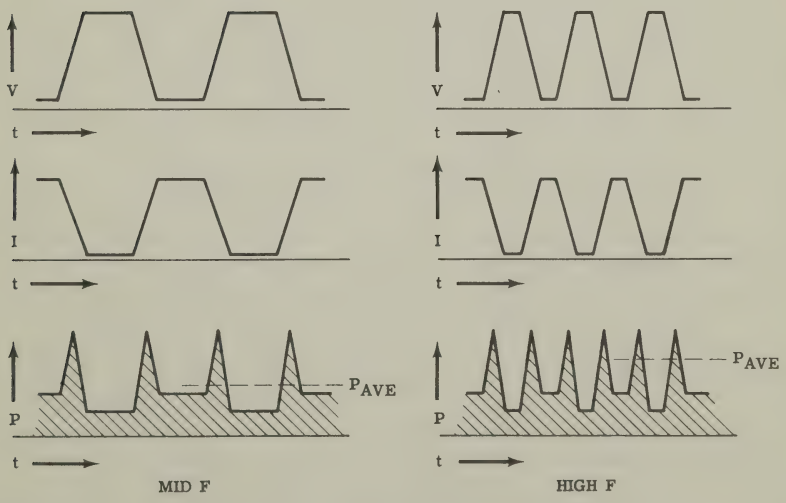


Figure 4-16 — Voltage, Current, and Power Wave Shapes Versus Frequency

Assuming I_{CBO} to be negligible during rise and fall intervals, this equation may be rewritten:

$$P_{ave} = \underbrace{\frac{1}{T}\int_0^{t_f}\left[V_{CS} + \frac{(V_p - V_{CS})t}{t_f}\right]\left[I_p - \frac{I_p t}{dt}\right]dt}_{\text{(Power loss during fall time)}} + \underbrace{\frac{1}{T}\int_0^{T/2 - t_f}[I_{CO}V_p]\,dt}_{\text{(Power loss during off time)}} +$$

$$\underbrace{\frac{1}{T}\int_0^{t_r}\left[V_p - \frac{(V_p - V_{CS})t}{t_r}\right]\left[\frac{I_p t}{t_r}\right]dt}_{\text{(Power loss during rise time)}} + \underbrace{\frac{1}{T}\int_0^{T/2 - t_r}[I_p V_{CS}]\,dt}_{\text{(Power loss during on time)}}$$

$$P_{ave} = \underbrace{\frac{I_p(V_p + 2V_{CS})\,(t_f + t_r)}{6T}}_{\substack{\text{(Switching loss — sum of rise} \\ \text{and fall losses)}}} + \underbrace{\frac{I_p V_{CS}}{T}\left[\frac{T}{2} - t_r\right]}_{\text{(On loss)}} + \underbrace{\frac{I_{CO}V_p}{T}\left[\frac{T}{2} - t_f\right]}_{\text{(Off loss)}} \qquad (4\text{-}7)$$

If rise and fall times are considered equal, the following simplification results:

$$P_{ave} = I_p\,[2t_r\,(V_p - V_{CS}) + 3V_{CS}T] + 3I_{CO}V_p\,(T - 2t_r) \qquad (4\text{-}8)$$

If two transistors with the same I_{CO} are being compared, the last term of the equation can be eliminated. Also, if $V_{CS} << V_p$, for comparison purposes we can write:

$$P_{ave} = \frac{I_p\,(2V_p t_r + 3V_{CS}t}{6T} = \underbrace{\frac{I_p V_p t_r}{3T}}_{\text{(High Frequency Loss)}} + \underbrace{\frac{V_{CS}I_p}{2}}_{\text{(Low Frequency Loss)}} \qquad (4\text{-}9)$$

Figure 4-17 is a plot of power loss vs square-wave frequency for two Motorola power transistors, each at two voltage settings. In a practical case a temperature measurement on a heat sink with a known thermal resistance will give an accurate indication of power loss.

4-4 — DC-to-AC Inverters and DC-to-DC Converters

A DC-to-AC inverter is a circuit designed to change a constant D-C voltage into a square-wave or sine-wave voltage; usually voltage step-up is employed. A DC-to-DC converter is an inverter with a rectifier stage added to produce a D-C output. These are shown in block diagram form in Figures 4-18 and 4-19.

Schematically the action of an inverter is represented in Figure 4-20. The two switches, S_1 and S_2, are ganged in such a way that if S_1 is closed S_2 is open, and vice versa. One method commonly used to operate switches is a mechanical vibrator, as illustrated in Figure 4-21. An electronic drive is outlined in Figure 4-22. Switching the voltage across the primary of the transformer yields a polarity change on the secondary as shown in Figure 4-20. The frequency of alternation will be determined by the square-wave drive. Since the polarity at the primary reverses during each half-cycle, the magnetic flux will also reverse and transformer action thus occurs. As one-half of the primary is energized, a voltage

equal to the battery voltage is induced into the open primary winding so that the off switch sees a back voltage equal to twice the battery potential, plus whatever inductive kick may be present.

The electronic inverter mechanical vibrator power supply can be replaced by an electronic transistorized inverter using a multivibrator to provide the necessary square-wave drive as shown in Figure 4-23. Design equations which apply to this application are listed in Table 4-1.

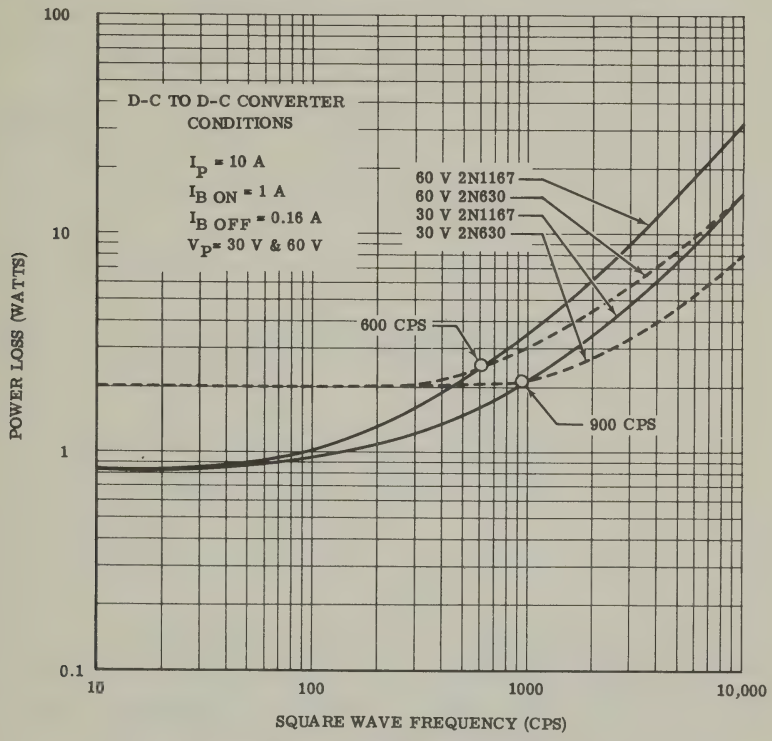


Figure 4-17 — Power Loss Versus Frequency

Figure 4-18 — Block Diagram D-C to A-C Inverters

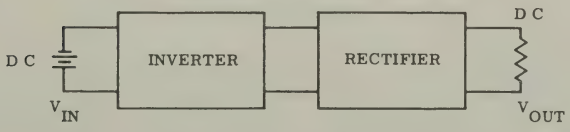


Figure 4-19 — Block Diagram D-C to D-C Converter

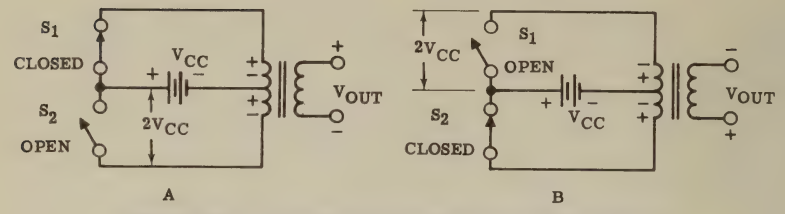


Figure 4-20 — Schematic Presentation of Converter

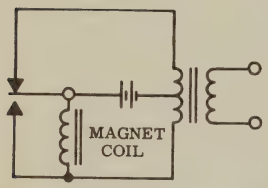


Figure 4-21 — Vibrator Method of Switching

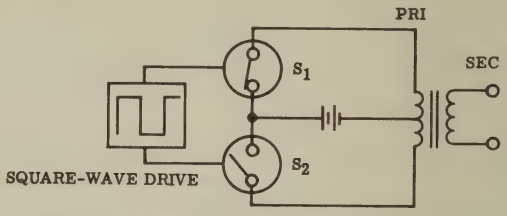


Figure 4-22 — Electronic Switch

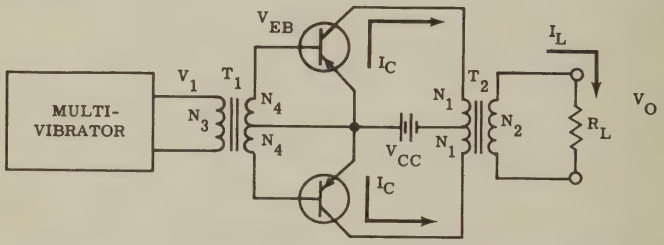


Figure 4-23 — Transistor Inverter with Multivibrator Drive

TABLE 4-1

Design Chart for Multivibrator Drive Inverter Transistor Switch (See Figure 4-23)

1. T_1 and T_2 must be capable of passing square waves.
2. T_1 must supply enough voltage to keep the transistor input saturated (full on) at the design load current.
3. $V_o = \frac{N_2}{N_1} V_{CC}$.
4. $I_C = \frac{N_2}{N_1} I_L$.
5. $I_L = \frac{V_o}{R_L}$.
6. $V_{BE} = \frac{N_4}{N_2} V_1$.
7. $g_{FE} = \frac{I_C}{V_{BE}}$

Resistor Coupled Inverter

The square-wave drive can also be obtained by feeding back part of the output into the transistor input, forming an oscillator. A cross-coupled resistor feedback oscillator is shown in Figure 4-24, with applicable design equations given in Table 4-2.

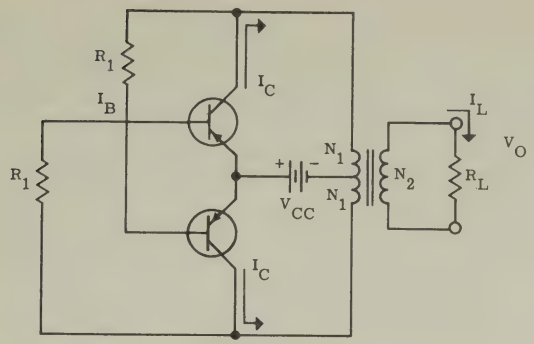


Figure 4-24 — Resistive-Coupled Transistor Inverter

TABLE 4-2

Design Chart for Resistor-Coupled Inverter (See Figure 4-24)

1. $I_B = \dfrac{2V_{CC}}{R_1}$
2. $I_C = \dfrac{N_2}{N_1} I_L$.
3. Choose transistor with adequate $h_{FE\ min}$ at 1_C.
4. Set forced gain (h_{FE} forced) equal to ½ $h_{FE\ min}$.
5. Therefore $I_B = \dfrac{2I_C}{h_{FE\ min}}$.
6. $R_1 = \dfrac{2V_{CC}}{I_B}$.

Single Transformer Inverter

Since the resistor-coupled feedback oscillator is somewhat inefficient and is difficult to control with regard to frequency, it is preferable to transformer-couple the feedback voltage, as indicated in Figure 4-25. Table 4-3 lists the design details for this type of inverter.

In the one-transformer saturable-core multivibrator, both the transformer and the transistor affect frequency of operation. Consider Equations 4-10 to 4-19 in Table 4-3. If either transistor is fully on, the whole supply voltage less $V_{CE\ sat}$ is across one-half of the primary, and the change of flux as a function of time must be constant to satisfy Equation 4-10. Thus the collector current, with no load, supplies an increasing magnetization current which generates the magnetic force. However, as the transformer approaches saturation, the incremental permeability, μ, begins to decrease and if the voltage is to remain constant the term di/dt must increase rapidly. This will cause a sudden spike of collector current which will be limited by the amount of feedback voltage into the base. This feedback voltage will begin to decrease as the magnetic coupling decreases due to saturation. The voltage across the transistor will move out of saturation and the voltage across the coil will be $V_t = V_{CC} - V_{CE}$. As V_{CE} increases, V_t decreases which means that the flux must decrease. As flux reverses it must

traverse a path determined by the B-H curve. However, the voltage across the on transistor decreases to zero very rapidly and will reverse as the other transistor begins to turn on because of the feedback voltage reversal. The time for this reversal is determined by the transistor response. As the second transistor switches the battery across the other half of the primary, the second half of the cycle begins. It is similar to the first half-cycle but with opposite polarity. The collector current wave shapes and the $I_C - V_{CE}$ load line are sketched in Figures 4-27 and 4-28.

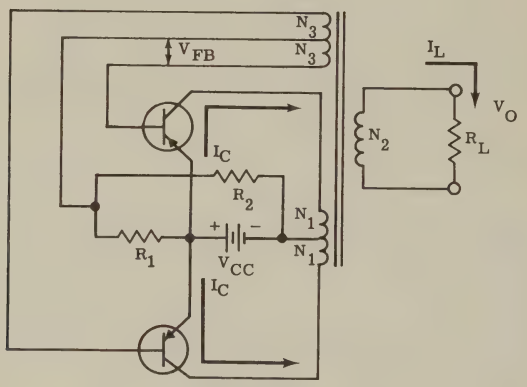


Figure 4-25 — Single-Transformer Inverter

TABLE 4-3

Design Chart for Single Transformer Inverter (See Figure 4-25)

1. $\dfrac{R_1 V_{CC}}{R_1 + R_2} = 0.3V,$

   (or experimentally determine necessary starting bias).

2. Find from data sheet minimum g_{FE} at I_C.

3. Determine necessary $V_{BE} = \dfrac{I_C}{g_{FE}}$.

4. Determine necessary $I_B = \dfrac{I_C}{h_{FE\ min}}$.

5. $V_{FB} = 2I_B \left[\dfrac{R_1 R_2}{R_1 + R_2}\right] + V_{BE}$.

6. $N_3 = \dfrac{N_1 V_{FB}}{V_{CC}}$.

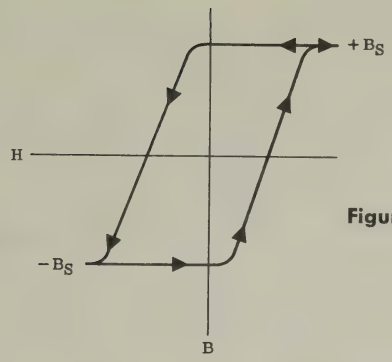


Figure 4-26 — Magnetization Curve

7. Formulas for saturable-core single transformer (see Figure 4-26),

$$V_1 = N_1 \frac{d\phi}{dt} \approx N_1 \frac{\Delta\phi}{T}, \tag{4-10}$$

$$\phi = BA \tag{4-11}$$

$$\Delta\phi = \Delta B \cdot A, \text{ and} \tag{4-12}$$

$$\Delta B = +B_s - (-B_s) = 2B_s. \tag{4-13}$$

$$\text{One-half cycle } \Delta T = \frac{1}{2f} \tag{4-14}$$

$$V_t = N_1 2B_s A 2f \tag{4-15}$$

$$f = \frac{V_t \times 10^8}{4B_s A N_1} \text{cps} \tag{4-16}$$

$$\mu H = B \tag{4-17}$$

$$H = Ni \tag{4-18}$$

$$V_t = (N_1)^2 \mu A \frac{di}{dt} \tag{4-19}$$

Where

i = magnetization current

V_t = voltage across one half primary ($V_t = V_{CC} - V_{CS}$)

μ = permeability

ϕ = magnetic flux

B = flux density (lines/cm^2)

B_s = saturated flux density

A = cross section area of core (cm)^2

H = magnetic force

N_1 = number of turns on one half of the primary.

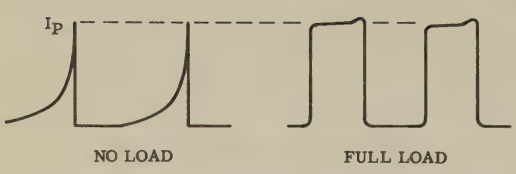


Figure 4-27 — Collector Current Wave Shape for One-Transformer Inverter

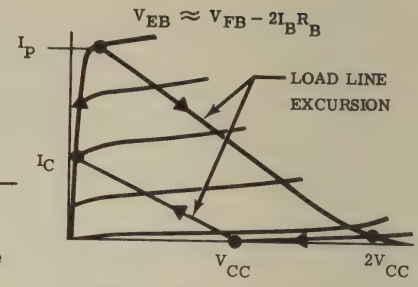


Figure 4-28 — Load Line of One-Transformer Inverter

Two Transformer Inverter

At large load currents it may be undesirable to saturate the output transformer since this will cause a high collector current spike. A two-transformer circuit which uses a low-power saturating transformer in the feedback loop is shown in Figure 4-29. The same conditions apply in this case as in the single transformer with the additional considerations listed in Table 4-4.

The no load and full load collector current wave shapes are similar to those shown in Figure 4-30. Notice there is no spike at no load.

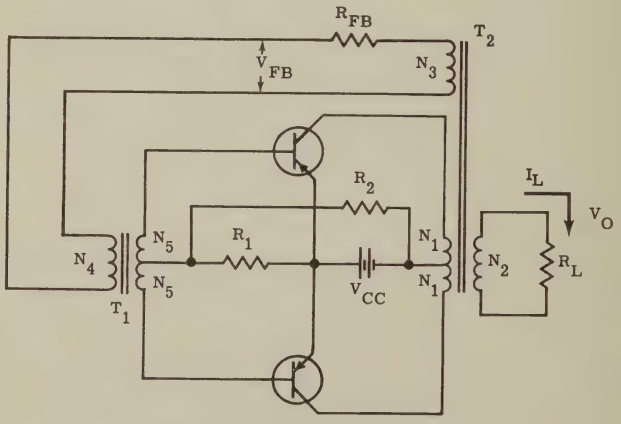


Figure 4-29 — Two-Transformer Inverter

TABLE 4-4

(See Figure 4-29)

Design Chart for Two Transformer Inverter (Same as Table 4-3 except):

1. T_2 must be designed to oscillate at least 10% lower in frequency than T_1.
2. $f = \dfrac{V_{FB} \times 10^8}{4N_4 A B_s}$.

Values are for driver transformer T_1, and note that the feedback voltage V_{FB} is used and not V_{CC}.

Figure 4-30 — Collector Current of Two-Transformer Inverter

Transformer Considerations

Inverters which operate at high frequency generally use ferrite core material. Silicon steel is used at 60 cps and 400 cps, two common frequencies. Tape-wound toroids are used where very high efficiency and quiet operation is desired. In any of these, leakage reactance must be held to a minimum to avoid voltage spikes. Load lines should be checked on the oscilloscope (see Section 2-17) to be sure that actual V_{CE}-I_C excursions are in the safe operating area for the particular device.

At high input voltages a bridge circuit similar to that shown in Figure 4-31 may prove useful. Assuming that there are no spikes, the V_{CE} will see the D-C supply voltage (V_{CC}), whereas in most transformer-coupled circuits V_{CE} will approach $2V_{CC}$.

The following sections illustrate specific switching circuit designs. Although most of the designs are common-emitter, it may be shown that any inverter circuit can be represented by one equivalent common-emitter circuit.

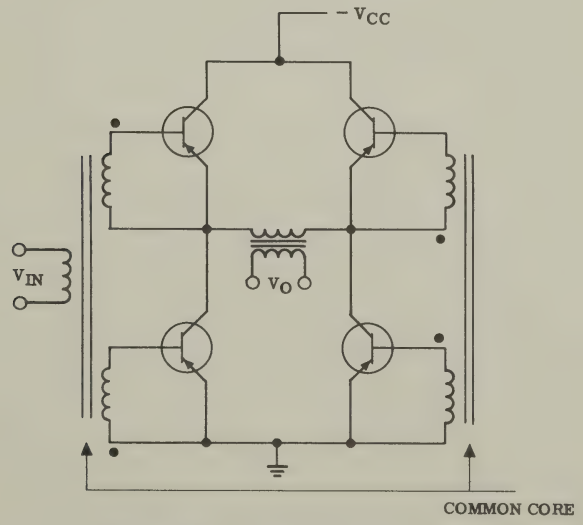


Figure 4-31 — Bridge Inverter

4-5 — 700-Watt Converter

POWER CONSIDERATIONS: The development of the Motorola 25-ampere 2N1162-1167 transistors opened new possibilities for efficient, high-current 28-volt converters. Since these transistors have a typical current gain of 25 at 25 amperes and transconductance of 25 mhos, it is apparent that a pair can efficiently switch 700 watts (25A × 28V). The saturation voltage at 25 amperes is approximately 0.3 volt, which means that during the on time about 7.5 watts will be dissipated in the collector-emitter junction. To allow for current-gain variations, about 2.5 amperes base drive is necessary to assure saturated conditions at all temperatures. Under these conditions about 1 volt appears from base to emitter. Thus nearly 2.5 watts is dissipated in the base-emitter junction during the on interval. This means that a pair of transistors would be dissipating an average continuous power of 10 watts.

So far it has been assumed that switching time is negligible. Actually a considerable power loss can occur during switching intervals. The rise and fall times in this converter are each about 50 μsec at 25 amperes, other circuit conditions are contributing to the rise and fall times. Calculations indicate that dissipation is increased by 25 watts (continuous) due to the switching times. Consequently a total of 35 watts is lost in the transistors.

With a heat sink, the case temperature of the transistors was 70°C when the ambient temperature was 25°C. This would indicate a junction temperature of about 84°C ($70°C + 0.8 \times \frac{35°}{2}$ C). However, the temperature kept increasing when power was on continuously, indicating the possibility of thermal runaway. A 10-CFM blower was used to stabilize the case temperature to below 60°C. The transistors were insulated from the heat sink with an anodized aluminum washer and silicone grease helped lower the thermal resistance from the transistor case to the heat sink.

TRANSFORMER AND CIRCUIT CONSIDERATIONS: A two-transformer design was used as shown in the diagram of Figure 4-32. This allowed the feedback transformer to do the saturating while reducing the collector current spikes. Since the output transformer does not saturate, the saturation losses were considerably reduced. However, the output transformer must still be able to faithfully transform a square wave and have reasonably low losses at heavy currents. The driver transformer was designed to oscillate from 200 to 1200 cycles with 2- to 12-volt drive. A multiple tap on the output transformer was wound on a double 4½" Hypersil C core, each half about ¾ of a square inch in cross section. The driver transformer consisted of three identical windings of #16 wire wound trifilar to provide various circuit configurations. The driver core was stack laminated of "mu" metal with a core area of about ⅜ of a square inch and about 1 × 1 × ½-inch outside dimensions. The circuit operated common-emitter push-pull. A 0.5-ohm potentiometer was inserted between the feedback winding and the driver transformer to allow proper switching action and help control the frequency. Performance was improved by inserting small resistors in series with the base. These 0.25-ohm resistors seem to equalize the drive and eliminate burnout problems. Since they do affect the frequency of operation (more voltage is required on the driver transformer), this factor must be taken into account.

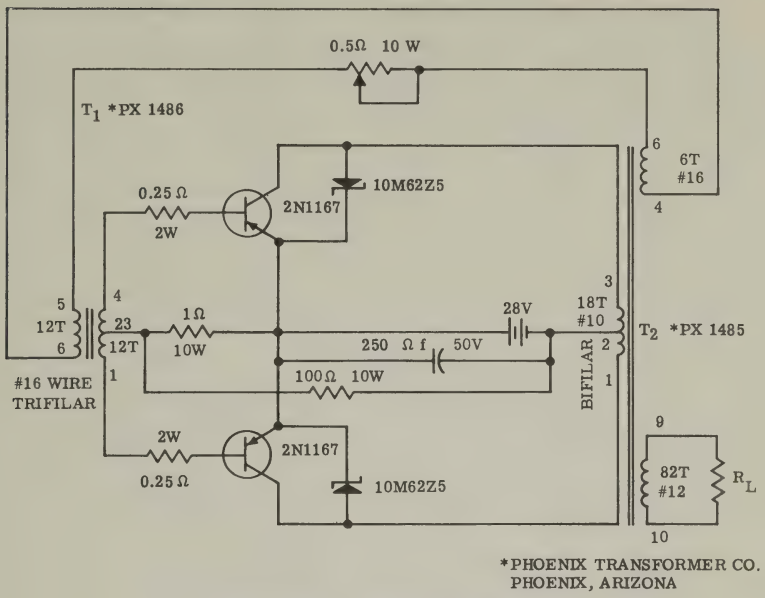


Figure 4-32 — 700-Watt Inverter

PERFORMANCE: From this circuit a power output of 575 watts was obtained with a power input of 700 watts, for an efficiency of about 82%. Bias and feedback resistors account for about 25 watts while another 35 watts was lost in the transistors. The other 65 watts apparently was lost in the transformers. An additional 20 watts was required to operate the blower, which was driven from the output. Currents of up to 34 amperes were switched and power outputs of more than 700 watts were obtained on an intermittent basis.

4-6 — An Efficient Two Stage DC-to-DC Converter

An efficient converter can be obtained by using a low-power, saturating oscillator to drive a high-power amplifier (Figure 4-33). This arrangement offers several advantages. The saturating transformer can be quite small since only a few watts of power need be handled. For this reason it is practical to use high-quality, rectangular-loop core material. The power transformer can be a conventional Class B pulse type with a silicon steel core, capable of passing a square wave with little distortion. A low-power audio transistor, such as the Motorola 2N176 for 12-volt operation or the Motorola 2N375 for 28-volt operation, fulfills the driver requirement.

Since the oscillator switches at low currents, the dangerous region of secondary breakdown can be avoided, eliminating the burnout problem. C_1, R_1, and C_2, R_2 form speedup networks to improve switching time. R_3 and R_4 are equalizing resistors which prevent excessive drive to high-gain units, and C_3 and C_4 are line filters. Matched output transistors should be employed. Switching time in the oscillator is 4 microseconds.

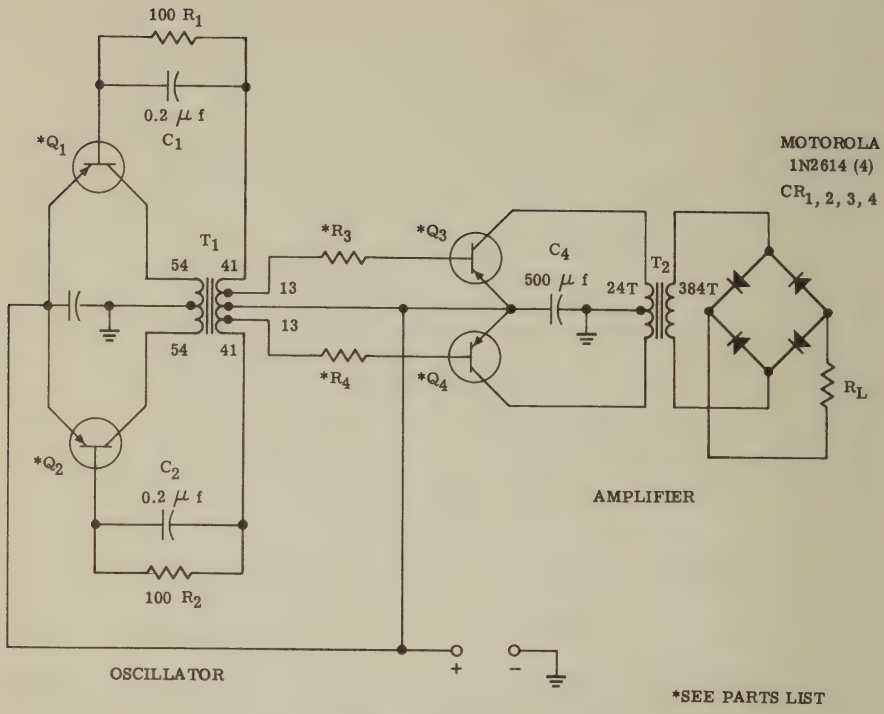


Figure 4-33 — Two-Stage Converter

The amplifier switches 10 amperes of collector current in 10 microseconds. As with similar circuits, the amplifier transistor must not be removed from the socket with the power applied, otherwise the resulting high-voltage spikes will damage the remaining amplifier transistor. If an excessive load is applied or if a short circuit occurs, the base drive will not hold the collector voltage at the saturation value and thermal damage may occur. The output should therefore be fused.

Efficiency of this circuit is shown in Figure 4-34.

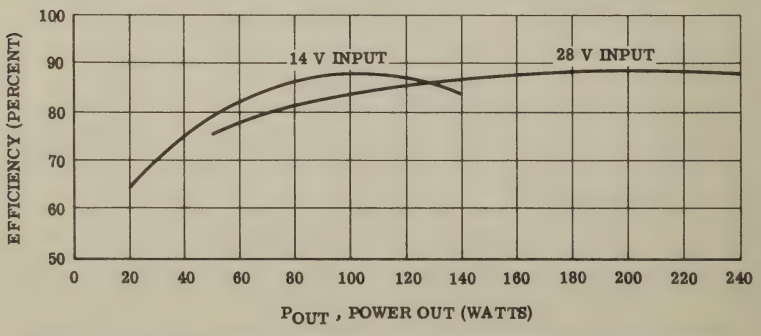


Figure 4-34 — Efficiency Versus Power Out for Two-Stage Converter

PARTS LIST FOR THE OSCILLATOR-AMPLIFIER CONVERTER CIRCUIT SHOWN IN FIGURE 4-33

D-C Input	D-C Output	Repetition Frequency	Q_1, Q_2	Q_3, Q_4	R_3, R_4
14V	200V	400 cps	2N176	2N627	0.5 ohm, 5W
28V	400V	800 cps	2N375	2N629	1.0 ohm, 5W

The following parts are independent of input voltage.

C_1, C_2 — 0.2 UF, 200V DC
C_3, C_4 — 500 UF, 50V DC
R_1, R_2 — 100 ohms, 1W
$CR_{1,2,3,4}$ — Motorola 1N2614
T_2* — MTR — 916 PX — 1301

TRIWEC TRANSFORMER CO. Chicago, Illinois or PHOENIX TRANSFORMER CO. Phoenix, Arizona

Transformer T_1: This transformer was wound on a Stackpole AP 11-424 Ceramag core and yoke with No. 22 Nyclad copper magnet wire. Bifilar winding was used. The primary has 108 turns and is center tapped. The secondary has 108 turns, with a center tap and with two additional taps 13 turns from each side of center.

*Transformer T_2 can be wound using the following material:

Material — Arnold Core Sectron 4 MIL C Core
AJ-H-12 Area = 0.5 sq. in. B_M = 12 kilogauss

When the oscillator is connected, the correct phase relationship between the primary and feedback windings must be maintained. If oscillation is not obtained and the phase terminals are not marked, reverse the collector or the base leads.

4-7 — Low Power DC-to-DC Converter Circuits

Figure 4-35 illustrates a circuit using Motorola power transistors and silicon rectifiers in conjunction with available converter transformers. Table 4-5 lists the components used.

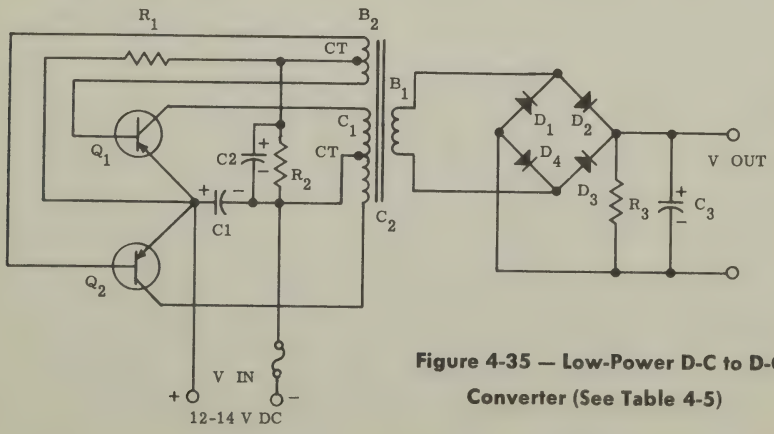


Figure 4-35 — Low-Power D-C to D-C Converter (See Table 4-5)

TABLE 4-5. CONVERTER COMPONENT RATINGS (See Figure 4-35)

Triad Transf. Type # or Equiv.	Rated Load Volts/mA	Q_1, Q_2 Motorola Power Transistor type (no. used)	$D_{1,2,3,4}$ Motorola Silicon H.V. Rectifier Type No.	R_1 Ohms/ Watts	R_2 Ohms/ Watts	R_3 Ohms/ Watts	C_1 μfd/ Volts	C_2 fd/ Volts	C_3 μfd/ Volts	Heat Sink Area Sq. In.	Efficiency at rated Load %
TY-68S	250/65	2N669 (2)	1N2613	500/5	50/5	300K/1	50/50	X	2/400	20	75
TY-69S	300/100	2N669 (2)	1N2614	10/5	150/2	300K/1	50/50	X	4/600	30	75
TY-70S	325/200	2N628 (2) or 2N176 (4)[a] or 2N669 (4)[a]	1N2615	10/5	100/5	300K/1	X	50/50	4/600	50	75
TY-71S	375/200	2N628 (2) or 2N176 (6)[b] or 2N669 (6)[b]	1N2615	5/5	50/5	300K/1	50/50	25/50	4/600	80	75

(a) Two transistors in parallel, each side.

(b) Three transistors in parallel, each side.

X = Not used.

4-8 — 50-Watt 110-Volt AC Source for Automobiles

This inverter (Figure 4-36) uses standard components. It has been designed to operate 110-volt equipment within its power rating from a 12-volt automobile electrical system (14-volts nominal). This inverter has been used to operate the following:

1. Electric Shaver
2. Dictating Machines
3. Fluorescent Desk Lamp
4. AC - DC Radio
5. "Pencil Tip" Soldering Iron
6. 40-Watt 117-Volt AC Trouble Lamp
7. Portable Phonograph.

Base bias and collector to base coupling is provided through resistors R_1 and R_2, which are 100 ohm, 2 watt. Bias stability is provided by the 15-ohm, 2-watt resistors R_3 and R_4.

The raw output from the secondary of T_1 is the waveform shown in Figure 4-37.

This inverter has a frequency output of approximately 60 cps and the peak-to-peak voltage (between the flat tops) is 250 volts at 50 watts. For applications 1, 3, 5, and 6, this output is satisfactory even though the waveform is approximately a square wave.

The hash filter, composed of C_1, L_1, and C_2, removes most of the spikes, giving a roughly trapezoidal wave form as shown in Figure 4-37B. This filter makes practical applications 2, 4, and 7. The frequency is reduced to about 56 cps by the filter.

With a 50-watt load the efficiency is approximately 75%. The voltage with a 50-watt load is about 106 volts.

The physical size of a completed unit is approximately 3 × 4 × 5 inches. Weighing about four pounds, it is provided with a cigarette lighter plug and a standard 110-volt outlet receptacle. Current drain with a 50-watt load is approximately 5 amperes.

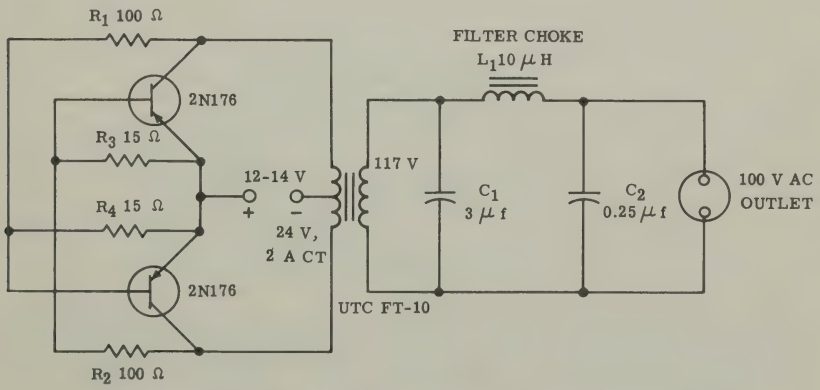


Figure 4-36 — Automobile 12-Volt D-C to 110-Volt A-C Inverter

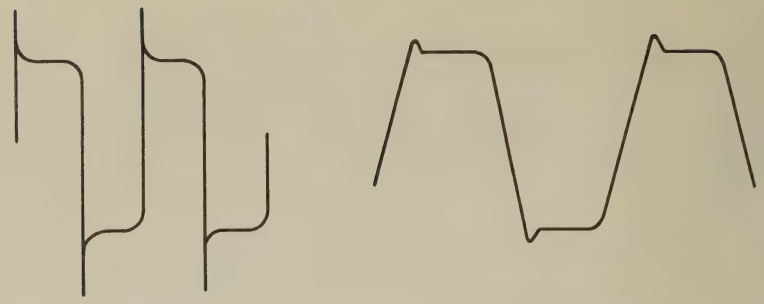


Figure 4-37 — Automobile Inverter Output Wave Shapes

4-9 — 400-cps 3-Phase Oscillator and Amplifier

A circuit to drive a 20-watt 3-phase load at 400 cps is shown in Figure 4-38. The 3-phase oscillations are supplied by an RC-coupled oscillator so that a 120° phase difference exists at the collector of each of the 2N651 transistors. An emitter-follower amplifier drives the output power transistors. The power transistors are driven into saturation, which provides a clipped sine wave on the secondary of the output transformer. This circuit has been used to drive a 3-phase aircraft gyro motor from a 12-volt D-C supply.

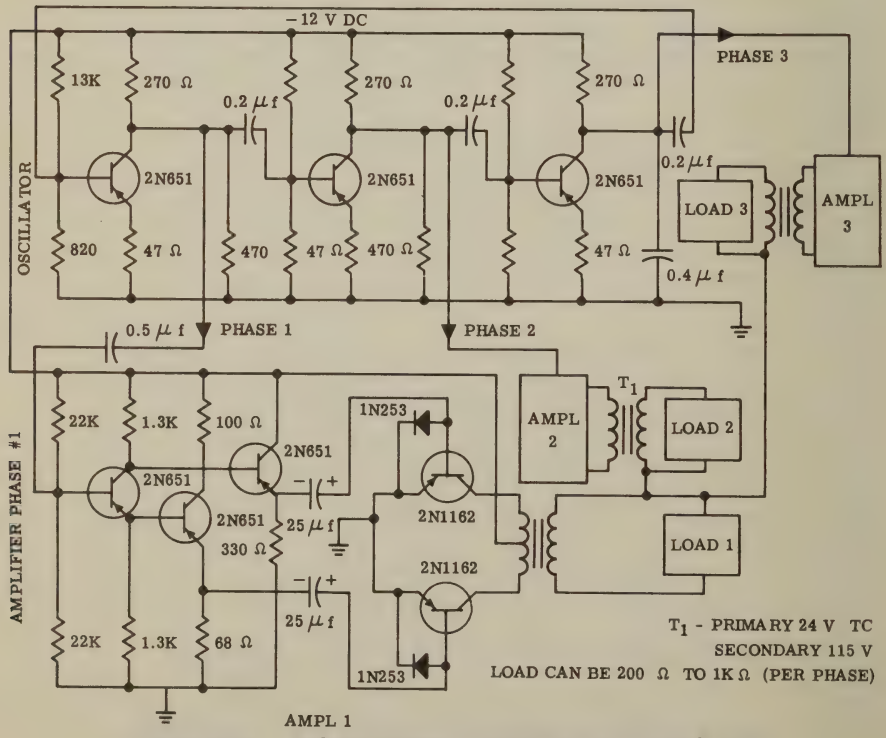


Figure 4-38 — 3-Phase Inverter, 12-Volt D-C to 115-Volt A-C

4-10 — DC-to-AC Variable Frequency Inverter

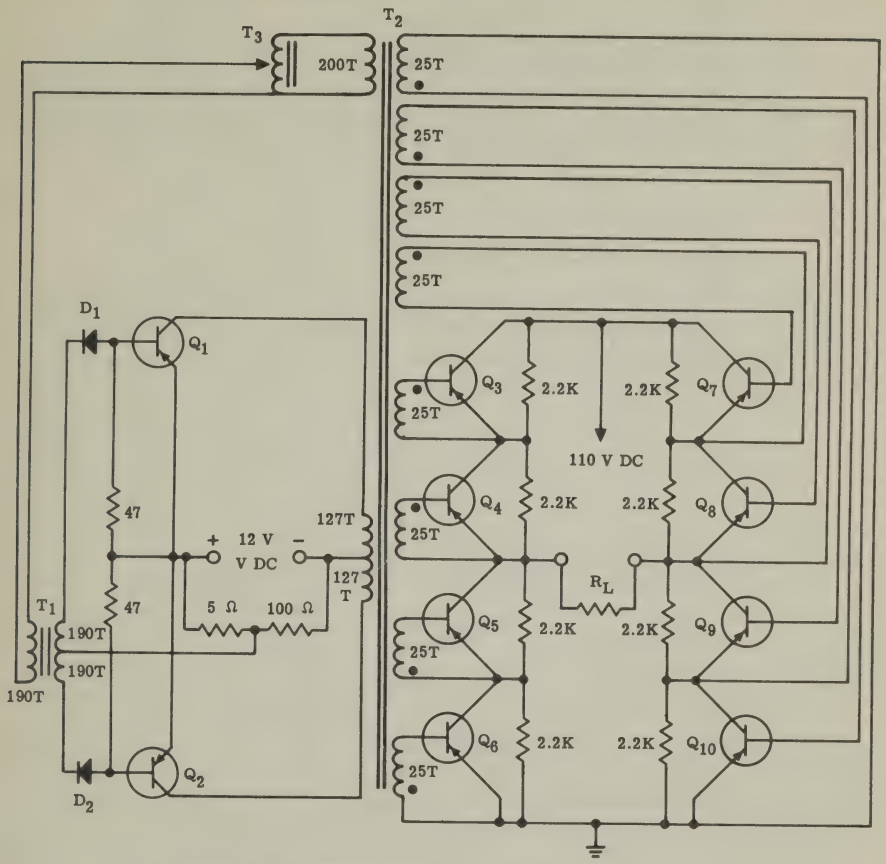


Figure 4-39 — Variable-Frequency D-C to A-C Inverter

PARTS LIST FOR FIGURE 4-39

D_1,D_2	—	50 Volt Silicon Diode Motorola 1N536
Q_1,Q_2	—	Motorola 2N1359
Q_3-Q_{10}	—	Motorola 2N1365
T_1	—	Core Stackpole Ceramag 20 Area 25/64 Sq. In.
T_2	—	Core Westinghouse Hypersil E17
T_3	—	Superior Type 10B Variable Autoformer

Many square-wave applications require a variable frequency output. One method of obtaining such an output is by using a two-transformer inverter to drive an amplifier, (Figure 4-39). The voltage across the input-saturating trans-

former is varied to change the frequency, as shown in Equation 4-16 which is repeated here.

$$f = \frac{V_t \times 10^8}{4B_s AN_1}. \tag{4-16}$$

The amplifier is a series bridge type. Swamping resistors are used to equalize the collector-emitter voltage of the series string. The output voltage is 110 volts at a square wave frequency of 20 to 200 cps. The input is 110 volts DC.

4-11 — 6-Volt D-C to 6-KV A-C Inverter

This application provides a high-voltage A-C or oscillatory output for driving gaseous luminous tubing. The output can be rectified and doubled to provide a 12-KV D-C source for cathode ray tubes.

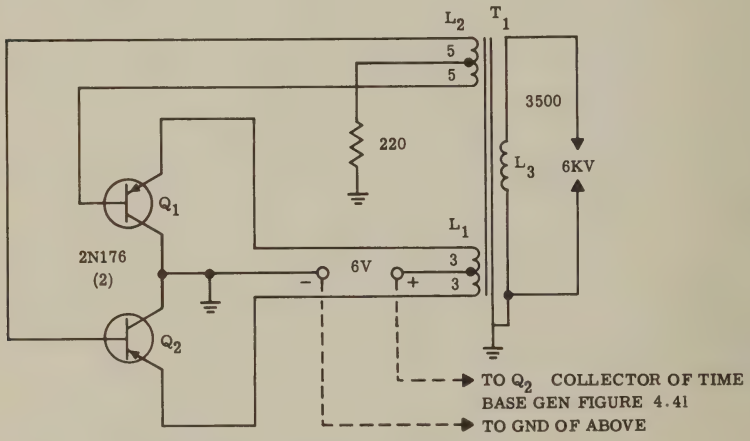


Figure 4-40 — 6-Volt D-C to 6 KV A-C Inverter

The circuit shown in Figure 4-40 differs from the inverters previously shown in that the common-collector configuration is used instead of a common-emitter. Consequently, transistors Q_1 and Q_2 need not be insulated from the chassis. This circuit also requires that the ratio of turns of L_2 (used for base drive) to L_1 be approximately 6:5.

SPECIAL OSCILLATOR TRANSFORMER T_1: Core Material: Ceramag U Cores — AP11-264 (2). Most TV flyback transformers are wound on a similar core, which can be used for this application.

L_1 and L_2 are handwound, side by side on the cardboard bobbin with taps brought out on either side. The winding is covered with 3 thicknesses of bond paper saturated with coil dope. L_3 is universal wound on this paper layer. The winding width is ¾-inch. After every 250 turns a layer of doped paper is applied to the winding. This is to add strength to the coil, which builds up to a diameter of approximately 2¾ inches. The coil is well doped, dried, and covered on the sides and top with masking tape painted with dope.

L_1 — 6 turns, C.T. #18 Nylclad

L_2 — 10 turns, C.T. #18 Nylclad

L_3 — 3,500 turns, #36 Nylclad, Silk

The inner lead of L_3 is grounded to any convenient point on the frame and the outer terminal brought out by a well-insulated lead.

Windings L_1 and L_2 must be correctly phased to obtain oscillation. Correct phasing is best established by trial and error. Reverse base leads if oscillation is not obtained on the first try. When this inverter is used in conjunction with the time base generator described below, an effective portable flasher unit is obtained which is capable of driving gaseous tubes for warning lights, flashing advertising signs, direction signs, and so forth.

4-12 — Power Drive Time-Base Generator (Flasher)

This is a self-running switch which delivers short burst of power (peak of 4-5 amperes) into a load at a repetition rate of a hundred times a minute. The actual repetition rate and the duration of the power bursts can be controlled over wide limits. A flashing warning light for traffic or construction hazards can be constructed using this time-base generator with a 6-volt incandescent bulb (such as a G.E. 1630) for the load.

A time-base circuit with a 6-volt supply is shown in Figure 4-41. This circuit consists of an NPN general purpose transistor (2N35 or equivalent) and 2N176 power transistor. This combination forms a negative-resistance relaxation oscillator whose period is controlled by the time constant of R_1C_1. Pulse duration increases as the value of R_2 is increased.

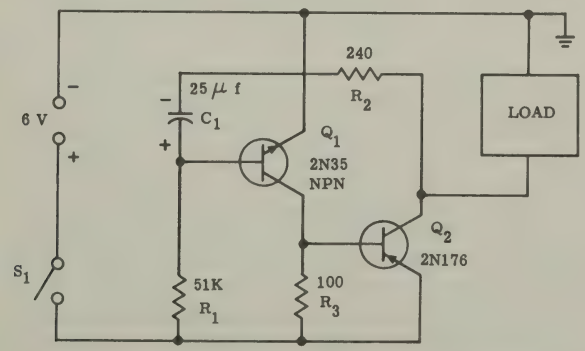


Figure 4-41 — Power Drive Time Base Generator

OPERATION: When switch S_1 is closed, capacitor C_1 starts to charge, raising the voltage on the base of Q_1 positive with respect to the emitter rate determined by the time constant of R_1C_1. At some critical voltage, Q_1 begins to conduct, followed by Q_2. When Q_2 is driven into saturation, practically the full battery potential is across the load. Conduction of Q_2 causes capacitor C_1 to discharge until at a low critical value Q_1 is cut off, causing Q_2 to cut off also. This action is repetitive and establishes the time base. The frequency of the circuit shown in Figure 4-41 is approximately 90 pulses per minute. Other time rates can be obtained by using different values of R_1 and C_1. Frequency varies inversely with the value of R_1 or C_1.

As the value of R_2 is increased, the pulse duration is also increased. In the circuit shown in Figure 4-41 the pulse duration is approximately 10 milliseconds. If the value of R_2 were increased to 1,000 ohms, the burst duration would be approximately 50 milliseconds.

The value of R_3 should be low to minimize I_{CBO}, a very small residual generated bias which could gate current into the load causing a standby power loss. However, the value of R_3 must be large enough so that it does not affect the saturation of Q_2 during the on period.

4-13 — Horizontal TV Deflection System

The circuit shown in Figure 4-42 shows how switching transistors are used in a transistorized horizontal deflection system for portable TV sets. Associated waveforms are shown in Figure 4-43. The current wave shapes were obtained by using a sampling system consisting of three 0.24-ohm wire-wound resistors in parallel.

Transistor Q_2 is turned on for approximately 48μs and off for 16μs by the voltage from the driver, as shown in Figure 4-43. For the first 9μs, collector current flows in the reverse direction because of the positive potential on the collector. After this initial 9μs it requires 39μs for collector current to build up to its peak forward value which is limited only by the inductance of the transformer and yoke. At the end of this period, base voltage goes positive, reducing base current to zero and causing collector current to fall to zero. This collapsing current induces a high voltage across the yoke and transistor during the retrace period. Capacitor C_4, in resonance with L_3, tunes this circuit to a frequency of $\frac{1}{2}t_r$, where t_r is the retrace time. As this voltage passes through 180 degrees and becomes positive, base current again flows and the cycle repeats. In the driver circuit, C_1 and L_1 form a resonant circuit at the third harmonic of the retrace frequency to reduce the peak voltage from collector to emitter. With this circuit, the peak voltage of 90 to 110 volts is reduced to 80 or 90 volts. This voltage reduction is only for the driver and has no effect on the output stage.

An advantage of using this circuit with transistors is that energy can be returned to the battery through bilateral action of the transistor, resulting in improved efficiency. At the end of the retrace cycle, the collector voltage begins to swing positive. Base and collector current will be high, limited only by the transistor saturation resistance and lead resistances. These currents decay rapidly to zero, however, because of the damping effect of the transistor on the free oscillations. Current then flows in the conventional manner. Thus part of the energy stored in the yoke during the forward sweep is returned to the battery.

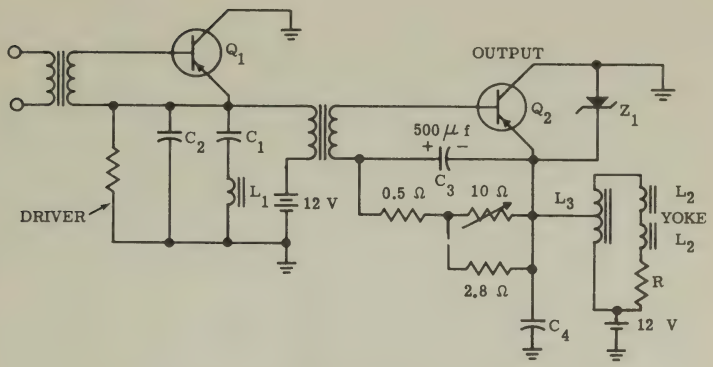


Figure 4-42 — TV Horizontal Output Deflection Circuit

TRANSISTOR REQUIREMENTS: The two important requirements of the output transistor Q_2 are high efficiency and the ability to withstand the high collector-to-emitter voltage. The Motorola 2N629 and 2N630 series fulfill these requirements. If the yoke is designed to give a higher voltage than the transistor can stand, a zener diode (10M91Z) can be used to clip the collector-to-emitter voltage to a safe level. An added precaution, however, is transistor protection afforded by the zener diode 10M91Z.

POWER CONSIDERATIONS: Figure 4-43D and 4-43C shows power dissipation as a function of time and emitter voltage during the fall time.

Assuming that the current and voltage relations are linear with respect to time, the following equation approximates the power dissipated during the off time.

$$P_F = \frac{V_{cp} I_{pf} (T_{to})^2}{(6_{t1})T} \qquad (4\text{-}20)$$

Reducing T_{to} by one-half reduces the power dissipated by a factor of 4. However, when switching time is reduced, the peak collector-emitter voltage is increased, so the inductance of the load may have to be reduced to limit this voltage pulse to a safe value.

High collector-to-emitter voltage can also be reduced by increasing the peak yoke and collector currents without degrading the deflection system.

The amount of deflection from a magnetic yoke is proportional to

$$D \propto \sqrt{I_{pp}\, V_{pp}}, \qquad (4\text{-}21)$$

where I_{pp} and V_{pp} are the peak current through and the peak voltage across the deflection yoke.

The circuit of Figure 4-42 supplies 600 volt-amperes to the yoke for 70°-90° deflection of a 14-inch tube.

With a peak-to-peak collector current of 8 amperes, 90 volts is required from collector-to emitter. If the peak voltage is reduced to 70 volts, collector current must be increased to 10.3 amps to maintain the same deflection.

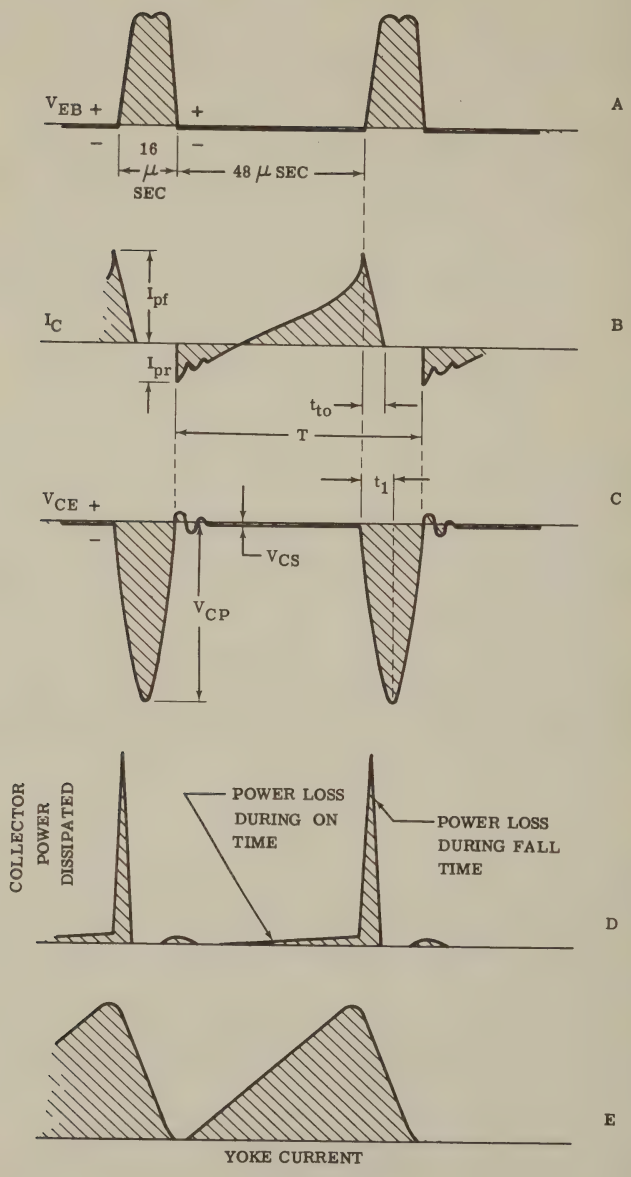


Figure 4-43 — Waveforms of TV Horizontal Drive Circuit (See Figure 4-42)

SERIES OPERATION: By operating two transistors in series, a much higher back voltage can be tolerated than is possible with a single transistor. Such a series arrangement is shown in Figure 4-44. A similar series arrangement is discussed in Chapter 6 on compound circuits. Germanium diodes D_1 and D_2 were used across each collector to emitter to increase the amount of reverse current flow during the first part of the sweep. These damping diodes decrease battery current by 100 ma from 1.7 to 1.6 amperes. A bifilar secondary winding on the input transformer is required to ensure equal drive to each transistor. If the drive is not equal, a voltage spike on the leading edge of the collector-emitter voltage waveform results, which could cause transistor failure.

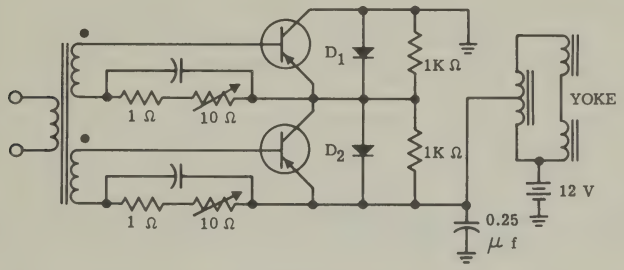


Figure 4-44 — Series-Connected Low-Voltage Transistors in TV Horizontal Output

The 1K resistors help balance the voltage across each transistor. In addition f_{ab} and C_{cb} should also be matched, so that nearly equal voltage division is obtained. Table 4-6 shows the results of matching pairs of the 2N629-630 series for various combinations of h_{FE}, f_{ab} and C_{cb}.

TABLE 4-6

	12 Volts Input			
Unit Number	h_{FE} 10 amps	f_{ab} 1 amp	C_{cb} 5V	Back Voltage
Q_1	20	288 kc	450 μμf	41V
Q_2	15	300 kc	450 μμf	43V
Q_3	16	256 kc	480 μμf	43V
Q_4	15	266 kc	485 μμf	41V
Q_5	16	261 kc	355 μμf	43V
Q_6	24	256 kc	350 μμf	40V
Q_7	17	279 kc	455 μμf	40V
Q_8	17	270 kc	460 μμf	43V
Q_9	13	282 kc	610 μμt	60V
Q_{10}	18	278 kc	460 μμt	45V
Q_{11}	25	259 kc	360 μμt	45V
Q_{12}	24	293 kc	535 μμt	60V
Q_{13}	16	248 kc	420 μμt	40V
Q_{14}	18	269 kc	420 μμt	55V

POWER LOSS & DEFLECTION EQUATIONS: Relations for power loss and beam deflection have been derived below as they relate to this transistorized deflection system:

1. Power Loss During Turn-Off (referring to Figure 4-43):

$$P_{to} = \frac{1}{T}\int_{o}^{t_{to}} V_C I_C dt \tag{4-22}$$

$$V_c = \frac{V_{CP} t}{t_i} \tag{4-23}$$

$$V_c = I_{PF}\left[1 - \frac{t}{t_{to}}\right] \tag{4-24}$$

$$P_{to} = \frac{V_{CP} I_{PF}}{t_i T}\int_{o}^{t_{to}} (t - t^2/T_{to})\, dt. \tag{4-25}$$

$$P_{to} = \frac{V_{CP} I_{PF} T_{to}}{(6t_i)T} \tag{4-26}$$

2. Amount of Electron Beam Deflection: For a given accelerating voltage and yoke configuration, deflection, d, is proportional to the peak ampere turns.

$$D \propto I_{pp} N \tag{4-27}$$

However, L, the inductance of the yoke, equals

$$L = kN^2, \tag{4-28}$$

so that $$D \propto I_{pp}\sqrt{L}. \tag{4-29}$$

During flyback, $$V_y = L\frac{di}{dt}. \tag{4-30}$$

Therefore, $$V_{pp} = \frac{2LI_{pp}}{t_r}, \tag{4-31}$$

and $$V_{pp} \propto LI_{pp} \tag{4-32}$$

where V_{pp} and I_{pp} are peak-to-peak values of voltage across the yoke and current through it, and t_r is the duration of the retrace.

Therefore $$D \propto I_{pp}\sqrt{V_{pp}/I_{pp}} \quad \text{and} \tag{4-33}$$

$$D \propto \sqrt{I_{pp} V_{pp}}. \tag{4-34}$$

CHAPTER V

Electronic Ignition Systems

5-1 — Introduction

The conventional ignition system, the basic design of which has remained virtually unchanged since first sketched by Charles Kettering in 1910, is one of the weak links of the modern internal combustion engine.

One disadvantage of this system is that the voltage output of the ignition coil decreases as engine speed increases, thus reducing the intensity of the spark produced by the individual spark plugs. This results in incomplete combustion of the fuel vapor-air mixture, causing inefficient engine operation and wasting gasoline.

Erosion of the points also occurs because of the high current flow each time the contacts open. This greatly reduces breaker point operating life.

While there have been minor improvements in points and ignition coils, resulting in a fair order of reliability, increased demands on the ignition system have more than offset these improvements. These demands are the result of more horsepower, faster engine speeds, higher compression ratios, and special fuels containing antiknock lead compounds.

As the overworked ignition system has been subjected to these additional demands, actual failures as well as a significant decrease in engine performance and efficiency have been unavoidable. The inconvenience of these failures has prompted considerable effort toward improving ignition system reliability.

Electronic systems have figured in these improvement efforts, but problems associated with electron tube circuitry (high plate voltages, warmup time, fragility) prevented progress in this direction. It required the recent great advances in the semiconductor industry to provide the devices necessary to realize the full potential of the electronic ignition system.

The use of semiconductor devices, such as power transistors, in electronic ignition systems offers many advantages. For example, the resulting circuitry is extremely rugged and requires no warmup time. It operates directly from normal battery voltages over a wide voltage range; an important consideration because of battery voltage drop during cold weather starting.

5-2 — Semiconductor Applications to Automotive Ignition Systems

There are three basic methods in which semiconductor devices can be used in automotive ignition systems. Each affords improvement over older systems both in performance and the life expectancy of ignition components. These methods are as follows:

1. Transistor Switching in the Conventional System
   The transistor handles the primary current. The breaker points carry only the transistor base current, resulting in less breaker point wear. The transistor itself is capable of switching much more current than simple breaker points.

2. Oscillatory Spark System
   Redesigned conventional or ferrite core transformers are used with power transistors in blocking or other oscillator systems to generate a high-voltage burst or pulse train. This may be either keyed for timing, or continuous, depending upon the application.
3. Capacitive Energy Storage System
   Although this method requires a relatively complex electronic system, it is very effective. The energy required to produce the high-tension output to fire the spark plugs is stored in the capacitor according to the relationship $E = 1/2\ CV^2$, as opposed to $E = 1/2\ LI^2$ in conventional systems where energy storage is provided by the inductance.

5-3 — Performance Requirements of an Ideal System

The end result of any ignition system is an electric spark. This spark must appear across the spark plug gap at exactly the right time in reference to the piston stroke and with sufficient power to ignite the fuel charge. Sufficient voltage must be available to ionize the spark gap.

The open circuit spark potential required for any engine is a function of several factors, and may range from 12 to 35KV. The peak spark power is approximately 900 watts for high-performance systems.

5-4 — The Conventional System

In the conventional, non-electronic system (Figure 5-1), a set of breaker points are alternately opened and closed by a cam geared to the motor crankshaft. On closure, a substantial primary current (4-6 amperes) flows into the primary coil, L_1, bringing the transformer core up to full magnetic saturation. This magnetic charging takes a little time, as represented by the rising curve of Figure 5-3A. When the breaker points are opened, the energy stored in the core induces

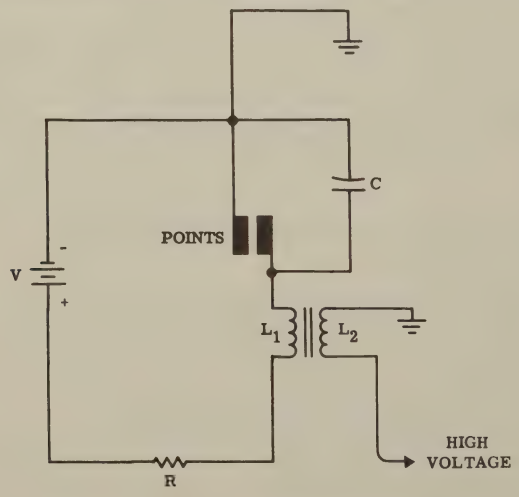


Figure 5-1 — Conventional Ignition System

a voltage ($e = L\ di/dt$) in the high-voltage coil, L_2, which depends on the rate of collapse of the magnetic field. This rapid collapse is augmented by the capacitor, C, which provides a low-impedance discharge path, and also reduces arcing between the points. The voltage generated across coil L_1 is stepped up by the turns ratio between coils L_1 and L_2. This ratio is usually on the order of 1:100 in standard 12-volt ignition coils. In conventional 12-volt systems, resistor R is used to lower the coil voltage.

5-5 — Transistor Switching

In a transistor switching circuit (Figure 5-2) the breaker points carry only the base current of the transistor, which is approximately 1/20 of the primary coil current. By reducing current through the breaker points this method eliminates burning and wear, and resultant mistiming. For this reason the transistorized system should be relatively maintenance-free.

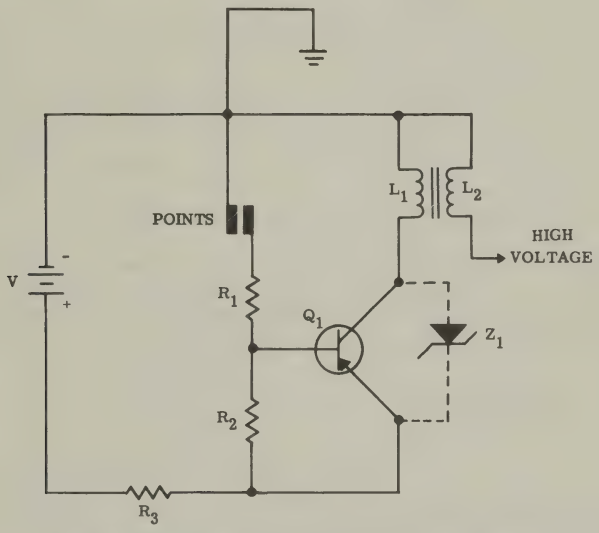


Figure 5-2 — Primary Coil Current Versus Time

During the interval after the breaker points open, a large reverse voltage appears across the primary coil and across the transistor. With a conventional 12-volt coil having a turns ratio of 1:100, 300 volts could be developed across the transistor at maximum output. This is the same high voltage that causes arcing and pitting of contacts in conventional systems. It is also capable of damaging the transistor unless some form of protection is provided.

One method of protecting the transistor is to install a zener diode across the terminals. The zener voltage should be somewhat less than the BV_{CES} rating of the transistor used.

By trading primary current for voltage it is possible to store in the coil the energy ($E = 1/2\ LI^2$) necessary to provide high output voltage, yet considerably reduce reverse voltage across the transistor. This is accomplished by designing

the ignition coil with a higher turns ratio. For example, special coils with 100 turns on L_1 and 30,000 turns on L_2 can be used to limit voltage across the transistor to 100 volts.

Current waveforms of Figure 5-3 show that the primary coil current increases to peak value much faster in the transistor system than it does in the conventional system.

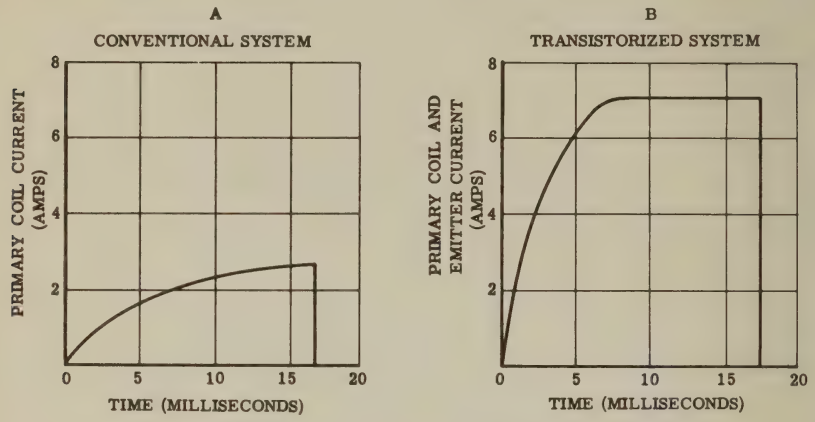


Figure 5-3 — Transistor Switching Circuit

The dramatic improvement in output voltage possible at higher engine speeds with the transistorized ignition system is shown in the curve of Figure 5-4. This is important because at these speeds high firing potentials are necessary, yet it is in this area that the output from conventional systems falls off rapidly.

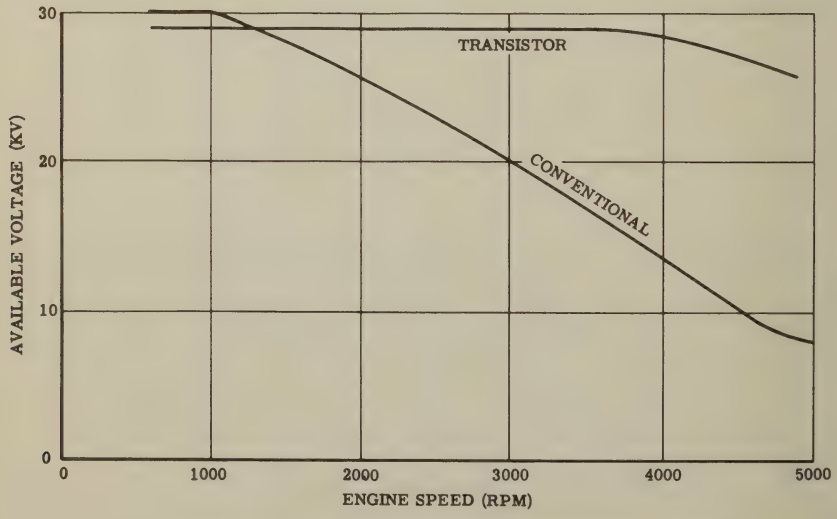


Figure 5-4 — Available High Voltage Versus Engine Speed

5-6 — High-Voltage Oscillator

A transistor can also be used to generate either a continuous or an intermittent source of oscillatory high voltage necessary to develop the ignition spark. This voltage can be obtained from a transistor blocking oscillator having a suitable ignition transformer. Suitable feedback is obtained from a standard or specially wound ignition coil. Coils with open silicon steel cores give oscillatory frequencies of 1 to 4 kc. Using closed ferrite cores, frequencies as high as 20 kc can be obtained. A feedback winding, L_3, (Figure 5-5) is provided on the ignition coil to obtain the blocking oscillation.

In an oscillator system, the protective considerations for the transistor are the same as in the switching system previously discussed; the coil should be wound to a turns ratio of 1:300 and zener diode protection should be provided.

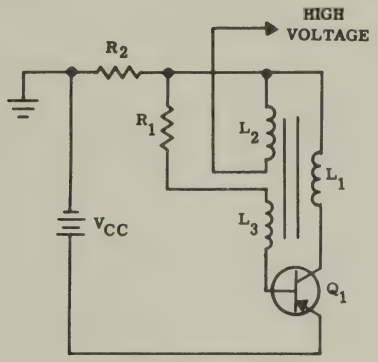


Figure 5-5 — Blocking Oscillator Ignition System

5-7 — Capacitor Storage System

A third system of producing a high voltage is the capacitor storage system, shown in Figure 5-6. In this system, a source of D-C voltage charges the capacitor, C_1, which is then abruptly discharged by a transistor, Q_1.

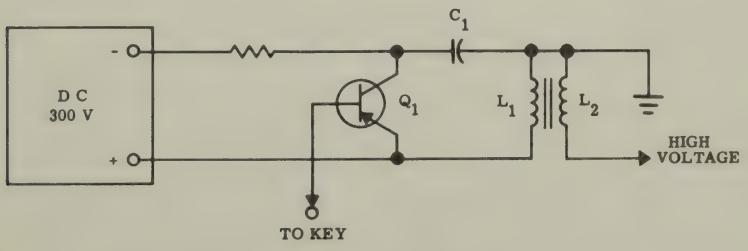


Figure 5-6 — Capacitor Storage Ignition System

The capacitive storage system gives a very hot spark from a standard ignition coil. The 300-volt D-C supply is obtained from a D-C to A-C inverter using two power transistors and a silicon diode bridge rectifier which converts the AC to DC. In this circuit, Q_1 sees the full D-C voltage of the supply as well as any high-voltage transients reflected back from the ignition coil. Therefore this system requires a transistor designed for this high voltage, or several in series as well as a protective zener diode.

This system is effective but it is relatively complex electronically and therefore perhaps less attractive than the transistor switching and oscillatory spark systems.

CHAPTER VI

Special Transistor Circuits

6-1 — Introduction

Appropriate parallel and series circuit arrangements of power transistors permit their use in high-voltage, high-current, or high-power applications. For example, power transistors have been used in parallel circuits to handle more than 1000 amperes and in series for more than 300 volts. That such applications are almost unlimited is indicated by one application in which 90 power transistors were used in parallel. Such circuits also insure reliability in extended areas of operation as well as yielding higher gain and lower distortion.

6-2 — Parallel Operation

Power transistors are used in parallel (Figure 6-1) to increase current- and power-handling capabilities. Since the number of thermal paths are also increased, this method allows greater power dissipation.

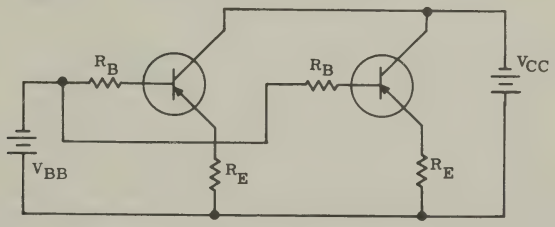


Figure 6-1 — Parallel Connection

To equalize collector current flow, the transistors should be matched or feedback resistors should be used to compensate for variations between individual units. Emitter resistors are generally used for current equalization because they also provide temperature stability. Current equalization can be obtained with a base resistor having a value equal to that of the emitter resistor times h_{FE}.

Either graphical or analytical methods can be used to determine the value of the emitter resistor required. The following example illustrates how a graphical analysis is used to determine the emitter resistance required. For this type of analysis the transconductance curves, which are emitter-to-base voltage, V_{EB}, versus collector current, I_C, are the most useful.

Consider the problem of matching a pair of Motorola 2N1165 transistors to handle a total current of 40 amperes. Each 2N1165 is rated for a maximum of 25 amperes. As the total transconductance variation is usually somewhat less than the total current gain variation, a transconductance ratio of 4:1 between minimum and maximum units will be used. This 4:1 ratio also takes care of normal temperature variations and aging characteristics. Figure 6-2 was constructed from this information and the information shown on the published data sheet.

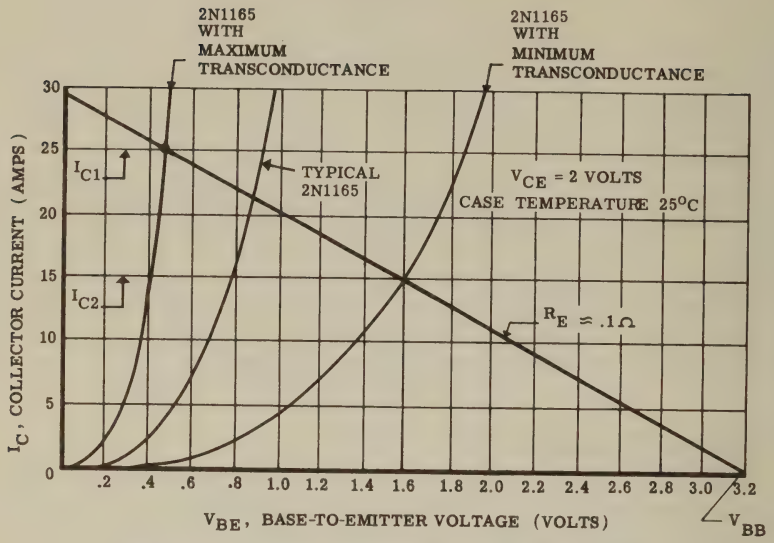


Figure 6-2 — Current Division by Emitter Resistor

In the example shown we have allowed the high-gain transistor to carry a maximum current of 25 amperes. This is the maximum collector current rating for the 2N1165. Since the total current to be handled is 40 amperes, the low-gain transistor must then carry 40 minus 25, or 15 amperes. A source resistance line connected between the 25-ampere point for the high-gain unit and the 15-ampere point for the low-gain unit gives us the required emitter resistance, approximately 0.1 ohm. The graph also shows that the required driving voltage, V_{BB}, for both units in parallel is approximately 3 volts. Because the 0.1-ohm resistance represents considerable power loss ($P = I_E^2 \times R_E$; $25^2 \times 0.1 = 62.5$ watts), it may be necessary to match transconductance of the units to obtain a higher efficiency. Although the use of a base resistor would reduce power loss as indicated by the following equation:

$$P = \frac{I_E^2 R_E}{h_{FE}} \qquad (6\text{-}1)$$

stability would be sacrificed to some extent.

6-3 — Series Operation

When a maximum voltage rating of a single power transistor is insufficient for a particular application, series operation is suggested (Figure 6-3). Various methods can be used to feed the base connections. Because of the high voltage existing between base connections, the base leads must be isolated from each other while sufficient drive is maintained. In the case of A-C or repetitive signals, simple transformer couplings can be employed (Figure 6-4). The transistors can be matched for transconductance, or the values of resistors R_1 and R_2 can be selected to balance the maximum voltage across each transistor. For most power transistor applications, R_1 and R_2 will be 10K.

Figure 6-3

Basic Series Connection

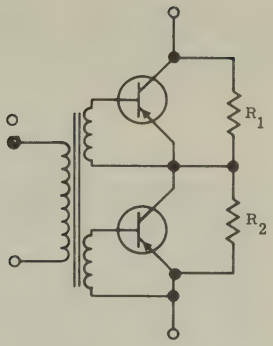


Figure 6-4

AC-Coupled Series Connection

The resistive driving network in Figure 6-5 is generally used for D-C voltage regulators. R_1, R_2, and R_3 are determined as follows:

$$R_1 = \frac{V_{CB}}{I_X + I_{CBO2} + I_{CBO3} - I_{B2} - I_{B3}} \tag{6-2}$$

$$R_2 = \frac{V_{CB}}{I_X + I_{CBO3} - I_{B3}} \tag{6-3}$$

$$R_3 = \frac{V_{CB}}{I_X} \tag{6-4}$$

In pulse-type circuits where the transistors are saturated in the on condition, the circuit in Figure 6-6 is not only more efficient but also offers greater thermal stability. In this circuit, terminals B, C, and E may be considered as

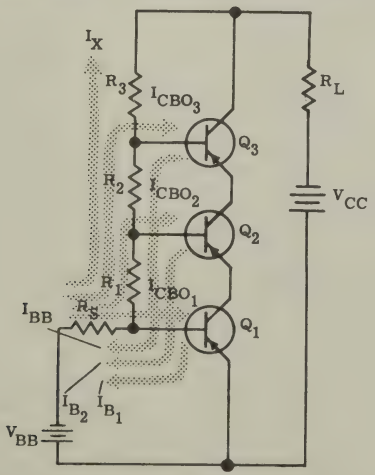


Figure 6-5 — DC-Coupled Series Connection

base, collector, and emitter terminals of a composite transistor. The zener diodes Z_1, Z_2, and Z_3 ensure that the maximum collector-emitter voltage of each of the series transistors is not exceeded.

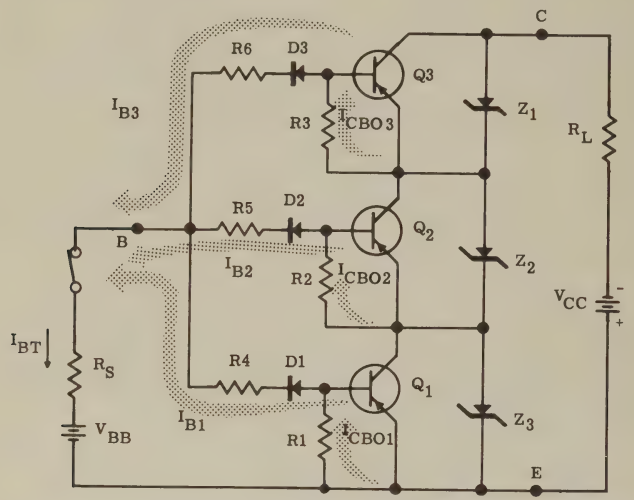


Figure 6-6 — Pulse-Type Circuit with Greater Thermal Stability

Resistors R_1, R_2, and R_3 provide I_{CBO} paths and ensure that the transistors will turn off under no-signal conditions. Decoupling diodes D_1, D_2, and D_3 permit a common driving signal to be used, because they open up in the absence of a driving signal and still permit the turn-on current to fully saturate each transistor. Resistors R_4, R_5, and R_6, used to balance out variations in gain between the series transistors, are determined as follows:

$$R_4 = \frac{V_{BB} - I_{BT}R_S - V_{D1} - V_{BE1}}{I_{B1}} \tag{6-5}$$

$$R_5 = \frac{V_{BB} - I_{BT}R_S - V_{D2} - V_{BE2} - V_{CE1\ sat}}{I_{B2}} \tag{6-6}$$

$$R_6 = \frac{V_{BB} - I_{BT}R_S - V_{D3} - V_{BE3} - V_{CE2\ sat} - V_{CE1\ sat}}{I_{B3}} \tag{6-7}$$

$$\text{where } I_{BT} = I_{B1} + I_{B2} + I_{B3}$$

In such a circuit the transistors operate in sequence and not simultaneously as in the other series circuits shown. When a signal is applied between base and emitter, Q_1 is turned on first and is driven to saturation before Q_2 begins to conduct. In turn, Q_3 is driven into conduction.

Better understanding of the Figure 6-6 series connection can be obtained by studying the following example. Figure 6-7 shows the collector characteristics of two Motorola 2N1166 transistors. Transistor A has a collector breakdown of 80 volts and Transistor B a breakdown of 70 volts. The collector characteristic of the two units in series is shown in Figure 6-8A. This Figure shows the composite collector breakdown to be 150 volts. Some nonlinearity can be observed

and a discontinuity appears between 40 and 70 volts where Transistor A begins to avalanche. The linearity of the composite transistor can be improved with feedback. The effect of a 1-ohm emitter resistor is shown in Figure 6-8B.

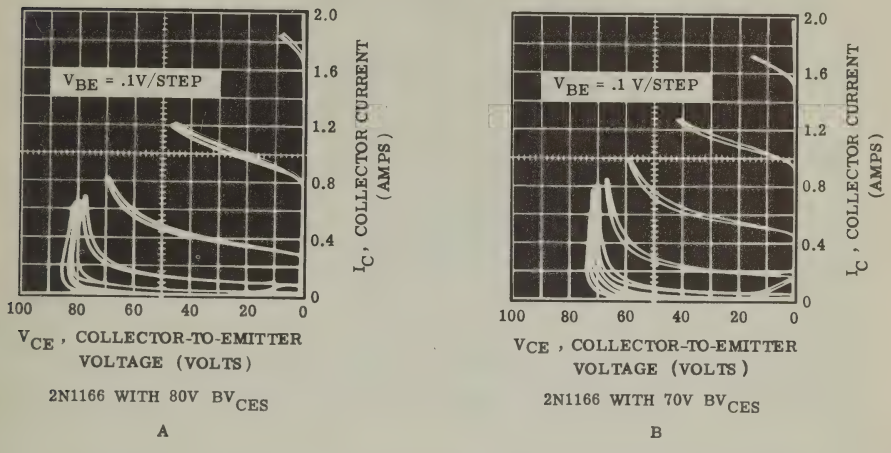


Figure 6-7 — Output Characteristics of Two Motorola 2N1164 Transistors

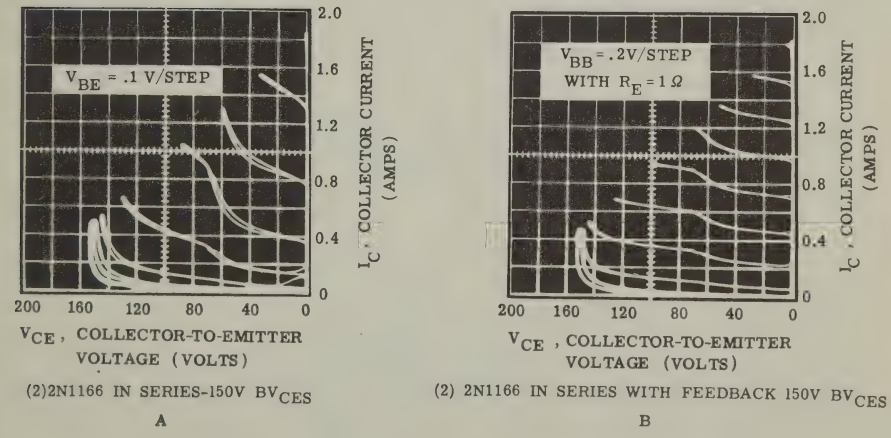


Figure 6-8 — Series Composite Output Characteristics of Two Motorola 2N1164 Transistors

Another important characteristic of this series connection is the higher saturation voltage, shown in Figure 6-9. This saturation voltage reaches 1 volt at 8.5 amperes, compared with a typical value of less than 0.2 volts for a single unit, without the 1-ohm emitter resistor.

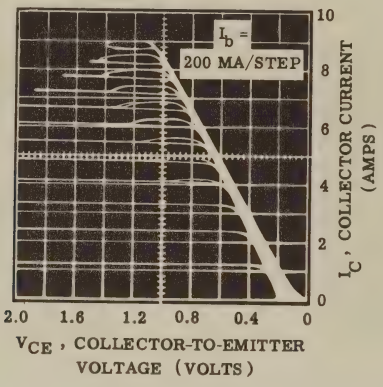


Figure 6-9 — Composite Collector Saturation Region of Two Motorola 2N1164 Transistors

6-4 — Compound Connections

Occasionally a current gain greater than that available from a single transistor is required and in some cases it is also desirable to provide improved linearity. By using two transistors in a compound connection (see Figure 6-10) the slope of collector current at high emitter currents will be significantly reduced. A disadvantage is that Q_2 cannot be driven into saturation. The common-emitter current gain of this connection is approximately the product of the gains of the two transistors. The emitter current of transistor Q_1 is the base current of transistor Q_2. Figure 6-11 shows the current gain linearity available from the compound connection.

Compound-connected transistors may be considered as a single transistor for design purposes. They can be used in complementary symmetry configurations of the push-pull and/or bridge arrangement.

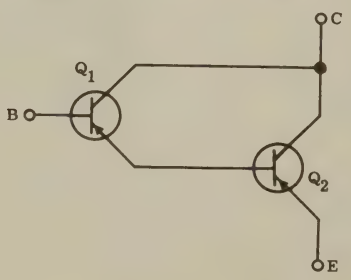


Figure 6-10 — Darlington Compound Connection

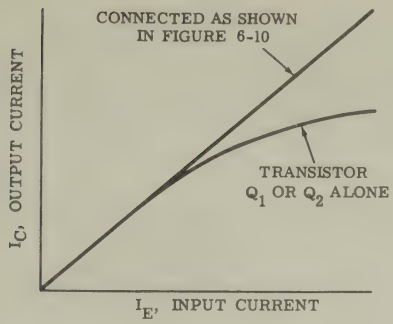


Figure 6-11 — Output Current Versus Input Current

Another compound connection, shown in Figure 6-12, uses a common-emitter input with a common-base output and floating battery connecting the collector of the first transistor with the emitter of the second.

This connection provides the current gain of the common emitter with the frequency and breakdown voltage characteristics of the common-base configuration. The floating battery can be as small as 2 volts, which permits the use of a transistor with a very low breakdown voltage for Q_1. The main disadvantage is that a separate battery is required.

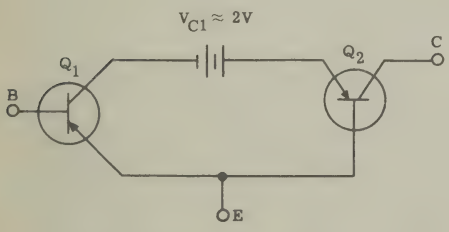


Figure 6-12 — Common-Emitter to Common-Base Compound Connection

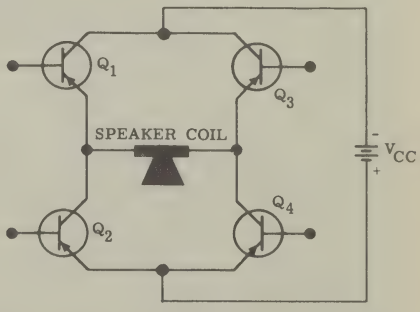


Figure 6-13 — Typical Bridge Connection

6-5 — Bridge Connections

The bridge circuit has advantages for two special applications. In audio applications, a speaker voice coil can be used as the load since no D-C current need pass through it. When the transistor is cut off it never sees more than the supply voltage, V_{CC}, whereas in a transformer-coupled push-pull circuit the transistor may see twice the supply voltage or more. Hence, with a bridge circuit, transistors can be used at higher voltages.

A bridge connection also eliminates voltage spiking problems in D-C to D-C converters since the battery or voltage source acts as a clamp that absorbs spikes. Figure 6-13 shows a typical bridge connection.

Junction Alloying of Power Transistors

CHAPTER VII

Power Supplies and Power Rectification

7-1 — Introduction

Power transistors find wide application for the following A-C power-supply functions.

1. A-C to D-C supplies (generally from 117-volt, 60-cps to low-voltage DC)
2. Controlled rectifiers
3. Electronic filtering and low-ripple supplies
4. Current and voltage regulation.

7-2 — Rectifier Characteristics of Germanium Power Transistors

The collector junction of a power transistor is an excellent diode for rectifying high currents at low voltages. The emitter junction also makes a good rectifier; however, due to thermal resistance considerations it is more practical to use the collector, or to tie the emitter and collector together. In practice, it is possible to use as a rectifier the same transistor that is being used in other parts of the circuit; for example, a 2-watt power output stage using Motorola 2N176 transistors can be supplied with 12 volts from a 2N176 used as a rectifier. Germanium power transistors used as diodes have excellent low voltage drop in the forward direction. Reverse breakdown is determined by resistivity in the base region (ρ_b) according to the following expression:

$$BV_{CBO} = 83.4(\rho_b)^{.61} \qquad (7\text{-}1)$$

where ρ_b is in ohm-cm and BV_{CBO} is in volts.

Typical forward and reverse V-I curves for Motorola power transistors when used as diodes are shown in Figures 7-1 and 7-2. Generally speaking, the forward characteristics are the same for the entire Motorola line. The remarkably low voltage drop is shown in Figure 7-1. Tests have shown that 25-50 amperes are needed before a one-volt drop is encountered. The reverse breakdown, of course, follows the voltage rating of the transistors and ranges from a low of 30 to a high of 120 volts for safe operation. The Motorola 2N1529 through 2N1560 series power transistors are not indicated but the BV_{CBO} rating given on the data sheet is the maximum voltage.

All Motorola industrial power transistors have a maximum junction temperature rating of 100°C. The load-current temperature-derating curve is shown in Figure 7-3. The maximum current rating is determined by the current carrying capacity of the base pin.

Germanium diodes are more efficient at high currents than selenium, silicon, or any of the metallic oxide rectifiers. With 100°C junction operation, back-to-front current ratios of 1000 to 1 and greater are possible at 10-ampere loads. Stacking units for higher voltage operation is possible with only a slight reduction in efficiency; stabilizing resistors should be "laddered" across the stack to equalize the reverse voltage. Parallel operation for higher load currents is no problem because of the uniformity of the forward V-I characteristic; however, current equalizing resistors may be needed.

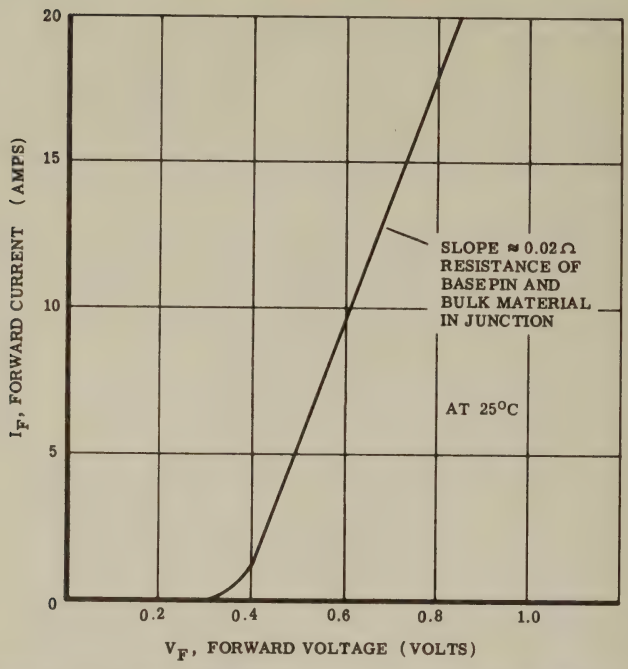


Figure 7-1 — Forward Diode Characteristics of Motorola Power Transistors

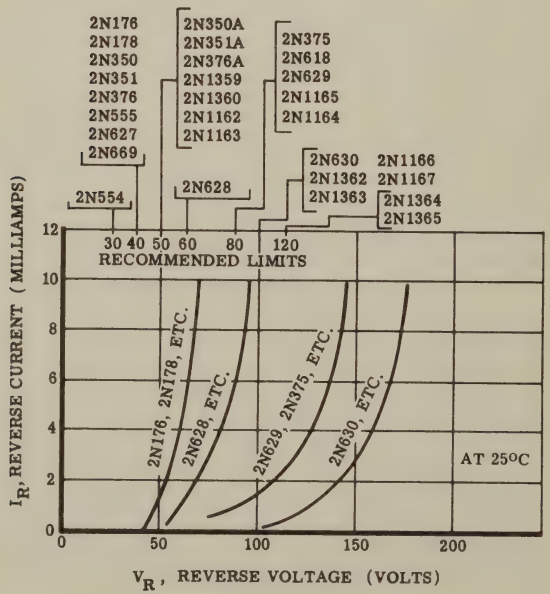


Figure 7-2 — Reverse Diode Characteristics of Motorola Power Transistors

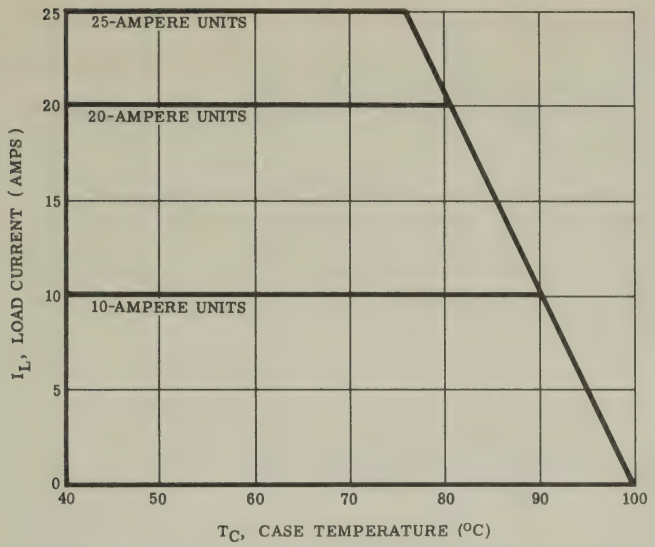


Figure 7-3 — Load Current — Temperature Derating Curve

7-3 — The Power Transistor as a General Purpose Rectifier

Power transistors can be used as rectifier diodes in any of the conventional rectifier connections such as half-wave, full-wave with center tapped secondary, bridge-type full-wave, doublers, and so on.

For these applications, the collector and base form the rectifying diode. The emitter is not used. Forward conduction occurs when the collector is positive with respect to the base. In conventional rectifier terminology the collector is the anode and the base is the cathode. The symbol designating a transistor used as a diode is shown in Figure 7-4.

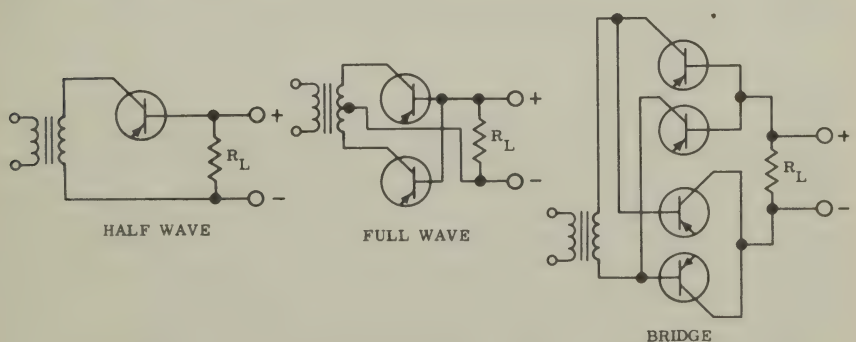


Figure 7-4 — Basic Rectifier Bridge Circuits Showing Transistor as a Diode

7-4 — Peak Inverse Voltage

Inverse voltage and power dissipation are the two principal ratings to be considered when setting up simple rectifier circuits.

The inverse voltage is a peak A-C value that may be as much as 2.8 times as high as the average D-C output.

Transistors may be connected in series for high-voltage applications with only a small voltage loss because of the low forward conduction.

An example of series-connected rectifiers operating as a 20-ampere half-wave rectifier at 117 volts AC is shown in Figure 7-5. For 117-volt line operation, the PIV of the four transistors in series must be approximately 400 volts. One-watt, 5000-ohm resistors are used to prevent the entire PIV from appearing across any one transistor.

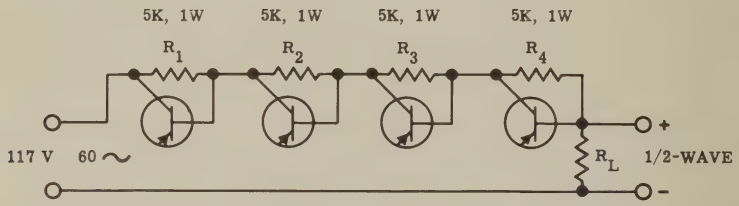


Figure 7-5 — Series Rectifier

Motorola power transistors used as rectifiers have small power loss because of the very low forward voltage drop. A conservative figure for rectifier power dissipation is 0.5 watt per ampere. For 2.5-ampere load current these transistors do not require a heat sink at room temperature. For a load current of 10 amperes a heat sink capable of dissipating 5 watts must be provided and at 20 amperes, 10 watts must be dissipated. The heat sink requirements are given in Chapter 2. In most equipment this heat sink requirement is satisfied by anchoring the transistors to a metal chassis or panel.

To handle more power (and larger currents) the units can be operated in parallel. Figure 7-6 shows five Motorola 2N627 transistors used as a 12-volt 100-ampere half-wave power supply. Center-tapped or bridge-type power supplies can also be designed in this manner.

7-5 — Power Control

Motorola power transistors offer unusual versatility and usefulness as power supply rectifier components in controlled current and voltage applications. A simple controlled full-wave rectifier circuit is shown in Figure 7-7.

In this circuit the current passed on each half-cycle is controlled by the value of R_C. Current is maximum when R_C is zero. The current through the transistor is limited by the load impedance, R_L. As R_C is increased, the base current to Q_1 and Q_2 becomes more and more limited, reducing the current applied to the load.

This results in a very smooth and effective control of output current and voltage into the load. Since R_C is carrying only the transistor base current, a 2- to 4-watt potentiometer can be used to remotely control load currents of several amperes. A battery charger using this principle is illustrated in Figure 7-8. The

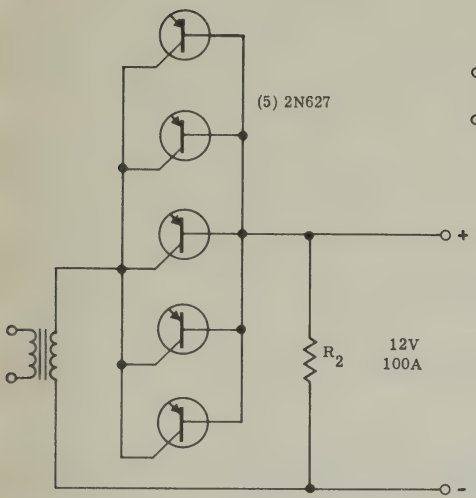


Figure 7-6 — Parallel Rectifier

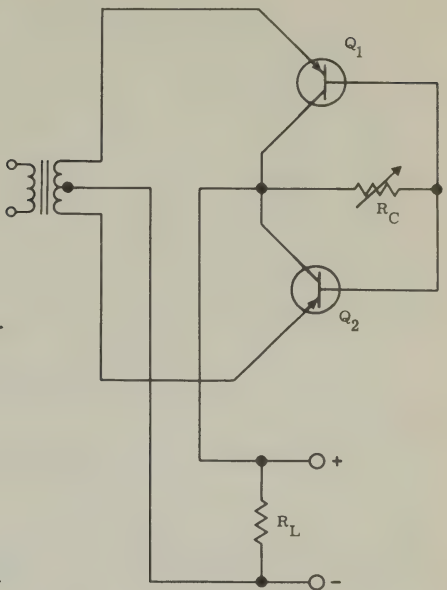


Figure 7-7 — Controlled Rectifier

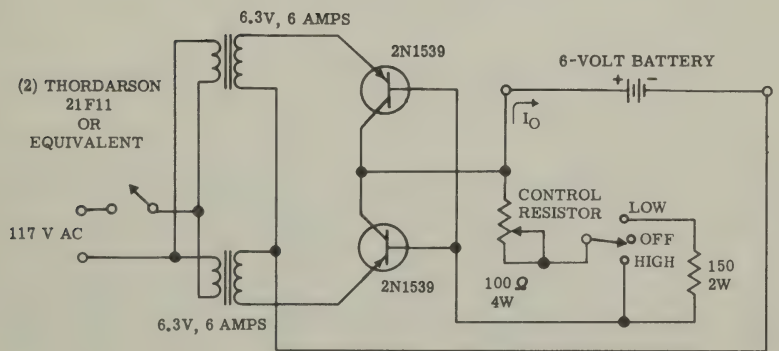


Figure 7-8 — Battery Charger

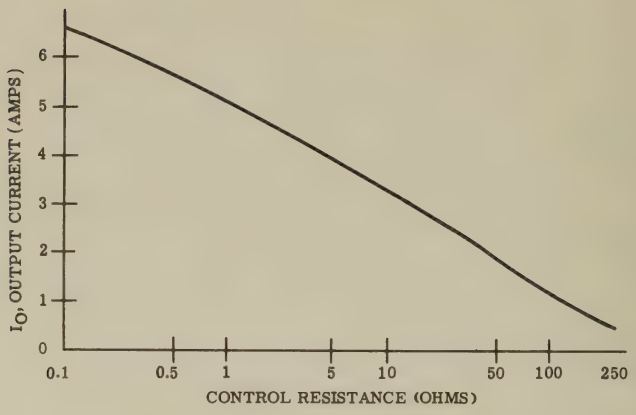


Figure 7-9 — Charging Rate Versus Control Resistance

variation in the output current of this supply as a function of control resistance and with a 6-volt storage battery as a load is shown in Figure 7-9.

7-6 — Electronic Filter *(Capacitance Multiplication)*

An electronic filter using a power transistor is very effective in reducing power supply ripple. An example is shown in Figure 7-10. The effective filter capacitance, C_F, appearing across the load is approximately

$$C_F = C_f h_{fe}, \tag{7-2}$$

where

C_F is the base filter capacitance, and
h_{fe} is the current gain of the transistor.

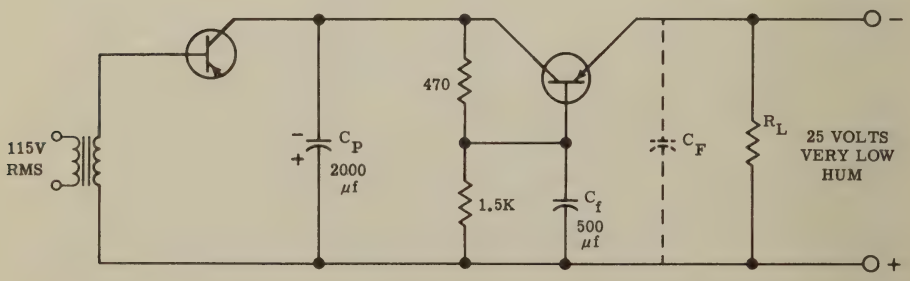


Figure 7-10 — Capacitance Multiplier

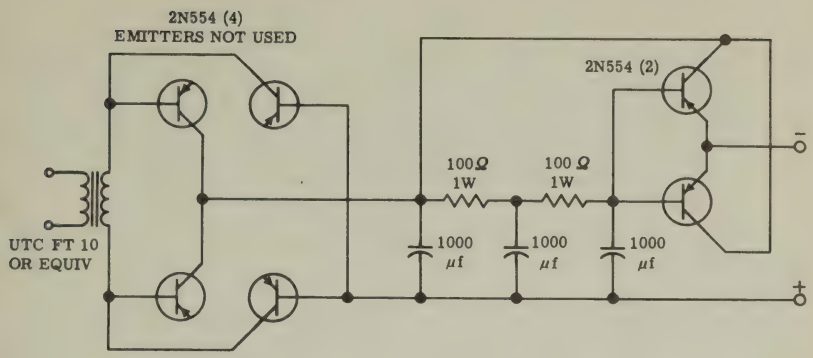


Figure 7-11 — Electronic Filter

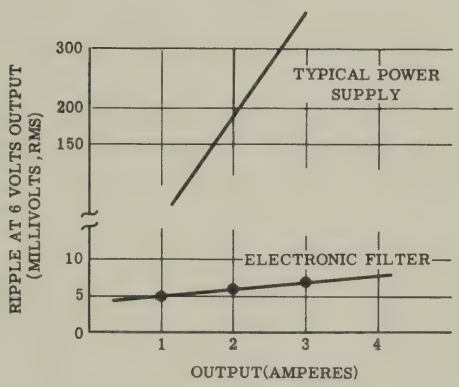


Figure 7-12 — Ripple Voltage Versus Output Current

This capacitance multiplying factor results in an effective C_F in the order of 25,000 microfarads in Figure 7-10 and about 160,000 microfarads in the circuit shown in Figure 7-11. The curves of Figure 7-12 were taken on the latter supply and show the very low ripple voltages obtained at high load currents. Equally effective filtering by the conventional choke-capacitance filter would require a very large and expensive inductor or capacitor for these currents.

This filter may be applied to almost any D-C voltage supply if the V_{CE} voltage is maintained low.

7-7 — Regulated Low Voltage Power Supplies

The use of zener diodes as control elements, reference elements, and filter elements in power supplies has been covered in the Motorola Silicon Zener Diode Handbook.

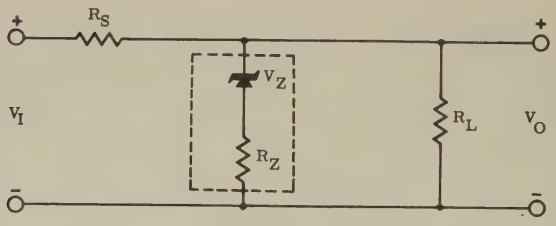


Figure 7-13 — Zener Shunt Regulator

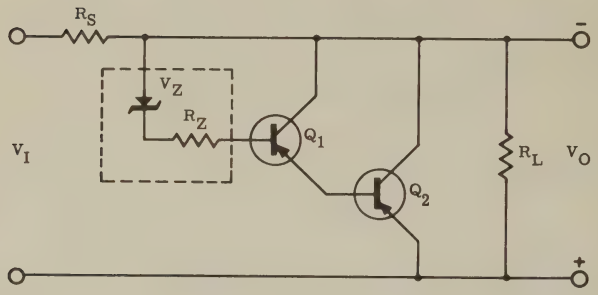


Figure 7-14 — Zener Shunt Transistor Regulator

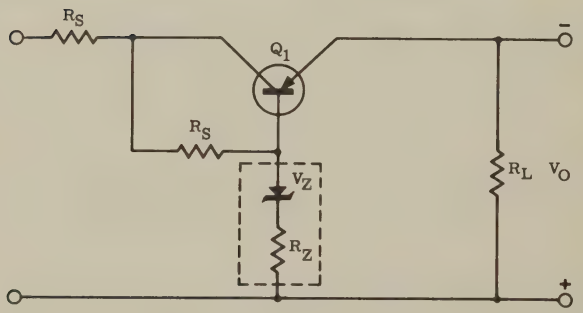


Figure 7-15 — Zener Series Transistor Regulator

The regulated supplies discussed take the form of the simple zener shunt regulator, Figure 7-13; the zener shunt-transistor regulator, Figure 7-14; the zener series-transistor regulator, Figure 7-15; and various zener-transistor combinations for feedback regulation, constant current, and high power regulation.

For complete information on regulated power supplies, including theoretical and design considerations, figures of merit and circuit analysis, the Motorola Zener Diode Handbook should be consulted.

A typical high-quality, high-power supply which features zener control of power transistor current handling elements, utilizing both positive and negative

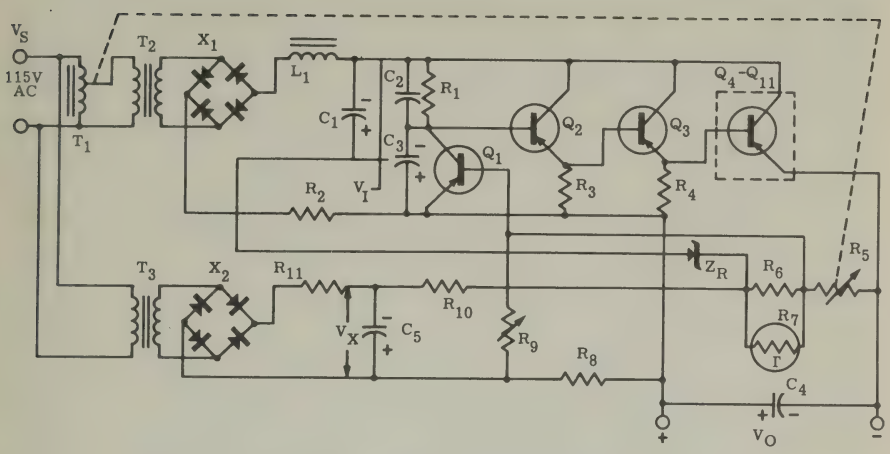


Figure 7-16 — Typical High-Quality, High-Power Supply

feedback to improve stability, is shown in Figure 7-16. This is an example of the power supply sophistication which can be obtained by using controlled power transistors.

Stabilization Bake

As a standard step in the manufacturing process, every Motorola Power Transistor is subjected to a 125° stabilization bake for 100 hours to stabilize units under accelerated life test conditions.

CHAPTER VIII

Transistor Testing

This section outlines the basic tests Motorola employs to ensure that a particular device meets its specification. The end use of the device determines the tests to which it is subjected. Production test equipment is naturally much more sophisticated than the simple circuits discussed here but the basic functions are the same.

COLLECTOR AND EMITTER CUTOFF CURRENT (I_{CBO} and I_{EBO}) may be checked with the circuit shown in Figure 8-1. The collector-to-base or emitter-to-base voltage should be set to the value indicated on the data sheet and the current read on a low-resistance meter. At room temperature and low voltages, readings will range from several microamperes to several milliamperes.

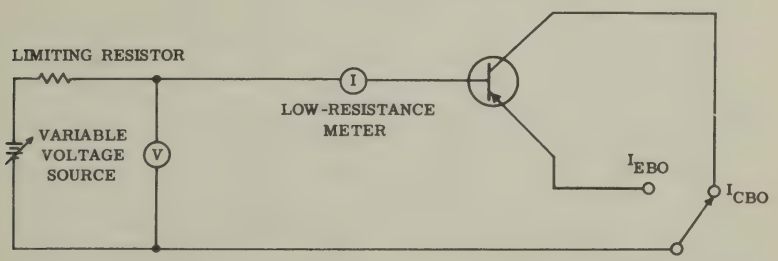


Figure 8-1 — I_{CBO} - I_{EBO} D-C Test Circuit

COLLECTOR BREAKDOWN VOLTAGE is generally measured with an oscilloscope sweep test. (See Figure 8-2.) This method avoids the excessive dissipation which is the disadvantage of a D-C test. The wave shapes of current versus voltage are described in Chapter 2. The variable sweep voltage is obtained with a

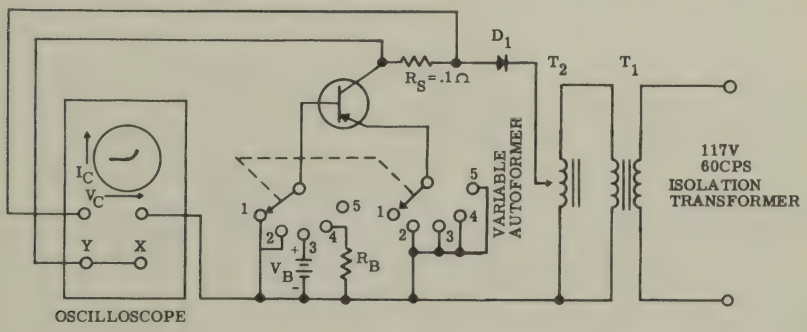


Figure 8-2 — Collector Breakdown Voltage Sweep Test Circuit

variable transformer, T_2, isolated from the line by transformer, T_1. The collector-to-common voltage is fed directly to the Horizontal Deflection Amplifier of the scope. The voltage developed by the flow of collector current through R_S is fed into the Vertical Deflection Amplifier. The five positions on the switch are for the following tests:

Position	*Function*	*Condition*
1	BV_{CBO}	Emitter Open
2	BV_{CES}	Base-Emitter Shorted
3	BV_{CEX}	$V_{BE} = +0.1$ Volt or greater
4	BV_{CER}	$R_B = 10$ ohms (value specified on data sheet)
5	BV_{CEO}	Base Open

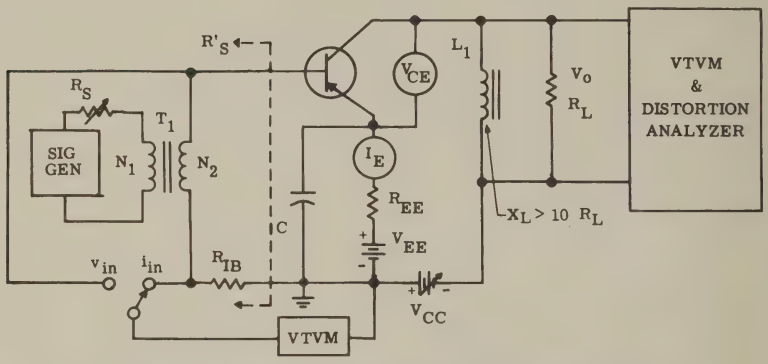


Figure 8-3 — Power Gain and Distortion Test Circuit

POWER GAIN AND HARMONIC DISTORTION must be tested in an audio circuit similar to that in Figure 8-3. The bias voltages and currents are adjusted to the values specified in the data sheet. The load resistance is also specified in the data sheet. The following adjustments are made:

1. Set I_E to data sheet value by adjusting V_{EE} and R_{EE}.
   $I_E \approx V_{EE} / R_{EE}$.
2. Set V_{CE} to data sheet value by adjusting V_{CC}.
3. Use value of R_L on data sheet by adjusting V_{CE} and I_E.

$$R_L \approx \frac{V_{CE}}{I_E}$$

4. Set drive impedance, R'_S, to data sheet value.

$$R'_S = (R_S + R_{GEN}) \left(\frac{N_2}{N_1}\right)^2 + R_{IB}.$$

5. Adjust signal input to get P_o given in data sheet. P_o can be measured directly by a power output meter (not shown) across L_1 or measured indirectly by using a VTVM to show desired v_o.

$$P_o = \frac{v_o^2}{R_L}$$

6. Measure harmonic distortion with distortion analyzer.
7. Calculate P_{in}

$$P_{in} = v_{in} i_{in} = v_{in} v_{RIB}/R_{IB}.$$

8. Calculate power gain in db; $G_e = 10 \log \frac{P_o}{P_{in}}$.

D-C CURRENT GAIN AND TRANSCONDUCTANCE are easily measured with D-C meters as indicated in Figure 8-4.

$$h_{FE} = \frac{I_C}{I_B} \text{ and } g_{FE} = \frac{I_C}{V_{BE}}.$$

At high currents, a heat sink may be necessary to dissipate power. Meter leads should contact transistor pins directly, rather than the socket or heat sink, to avoid measurement of voltage drop across the pin-socket connection.

Since $h_{FE} + 1 = \frac{I_E}{I_B}$ or $h_{FE} = \frac{I_E}{I_B} - 1$, D-C current gain can also be determined by adjusting V_{EE} and R_{EE} to give desired value of I_E and then measuring I_B. The current gain then equals $\frac{I_E}{I_B} - 1$.

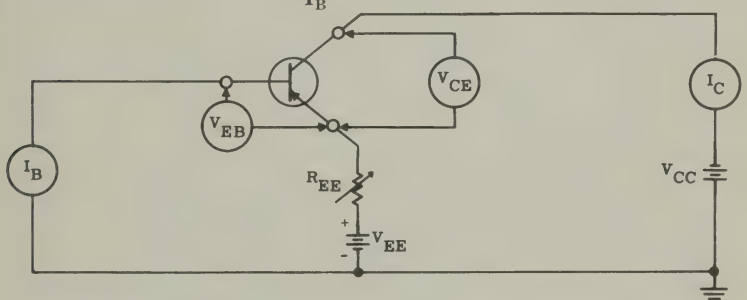


Figure 8-4 — D-C Current Gain and Transconductance Test Circuit

SMALL SIGNAL CURRENT GAIN, INPUT RESISTANCE, AND FREQUENCY CUTOFF (COMMON EMITTER) can be measured on the test setup shown in Figure 8-5.

$$h_{fe} = \frac{i_c}{i_b} = \frac{v_o/R_c}{v_g/R_s} = \frac{v_o R_s}{R_c v_g}.$$

The collector load resistor, R_c, should be very small compared with the transistor output impedance so that short circuit output is approximated. The value of R_s is made many times larger than the h_{ie} of the transistor. The value of v_g is then set to provide a small A-C value for i_b (approximately 50 microamperes), using the equation $i_b = v_g R_s$. L_1, C_1, and C_2 are used to isolate A-C and D-C effects. Then v_o is measured and substituted in the equation

$$h_{fe} = \frac{v_o R_s}{R_c v_g}.$$

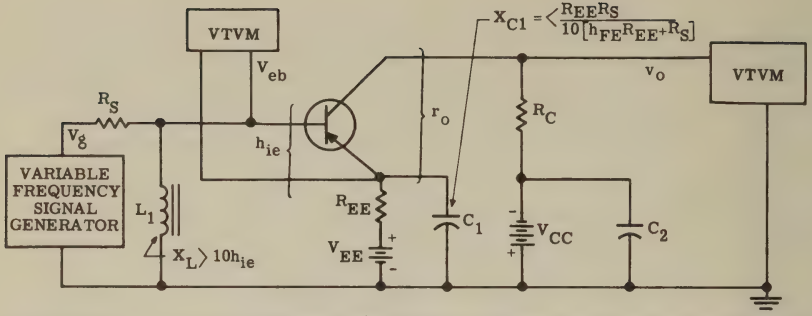


Figure 8-5 — Common-Emitter Small Signal Current Gain, Frequency Cutoff, and Input Resistance Test Circuit

The meter can be calibrated to read current gain directly as a function of v_o.

Input resistance is determined by using the circuit in Figure 8-5 with the same circuit values as used to determine h_{fe} and the equation

$$h_{ie} = \frac{v_{eb}}{i_b} = \frac{v_{eb}R_s}{v_g}.$$

v_{eb} is measured and substituted in the above equation. The meter can be calibrated to read h_{ie} directly as a function of v_{eb}.

Common-emitter frequency cutoff is found by adjusting the signal level to a convenient v_o at a low frequency and then increasing the signal frequency (holding v_g constant) until v_o drops to 0.707 of its original value. The original or reference frequency is given on the data sheet and is usually 1 kilocycle.

SMALL SIGNAL FREQUENCY CUTOFF (COMMON BASE) — Frequency cutoff (common base) is a more difficult measurement than the common-emitter configuration. The circuit in Figure 8-6 can be used. Because the frequencies usually lie between 100 and 1000 kc, proper wiring techniques must be observed. The common-emitter current gain, h_{fe}, will be equal to about 2.4 at the $F\alpha_b$ frequency and the input resistance, h_{ib}, will be in the order of several ohms at $I_E = 1$ ampere. Thus the isolating network should be about 100 ohms. To avoid D-C power loss, an R-F choke is usually inserted as shown in Figure 8-6.

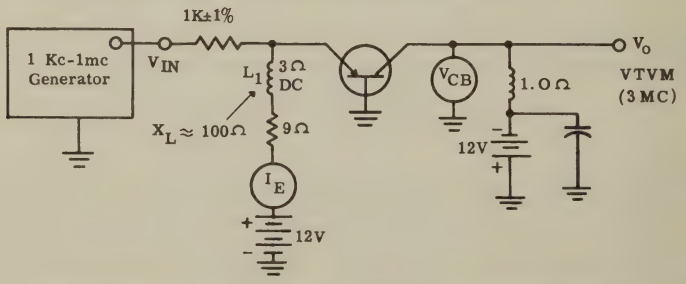


Figure 8-6 — Common-Base Frequency Cutoff Test Circuit

SATURATION VOLTAGE of the collector is generally tested under a forced gain condition using the test setup in Figure 8-7.

Using an arbitrary value of V_{CC}, adjust I_C to the value in the data sheet

by selecting the appropriate values of R_{CC}; $I_C = \frac{V_{CC}}{R_{CC}}$. Similarly, I_B, as given on the data sheet, is obtained by proper selection of the value of R_{BB}; $I_B = \frac{V_{CC}}{R_{BB}}$. $V_{CE\ sat}$ is then read directly. The meter leads should contact the transistor pins directly, rather than the socket or heat sink, to avoid measurement of voltage drop across the pin-socket connection. In the "worst case" situation, saturation voltage is read with the base shorted to the collector, and no forced gain exists.

Example: With a 2N627, a convenient $V_{CC} = 12$ volts, collector current $= 10$ amperes, and base current $= 1$ ampere. Then $R_{CC} = \frac{12}{10} = 1.2\Omega$, and $R_{BB} = \frac{12}{1} = 12\Omega$.

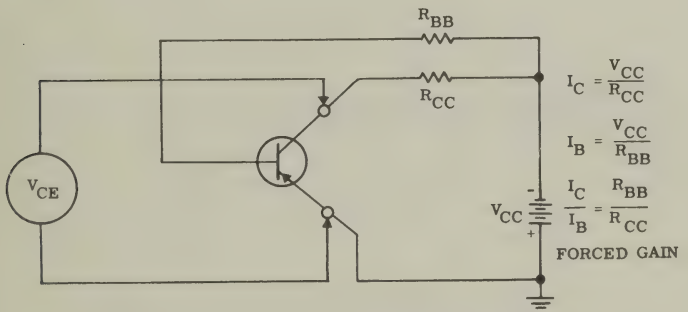


Figure 8-7 — Saturation Voltage Test Circuit

THERMAL RESISTANCE of power transistors can be tested in several ways using a test setup such as that shown in Figure 8-8. The basic method is to dissipate a known amount of power and measure the case temperature with a thermocouple. Then the power is abruptly removed and a temperature-sensitive

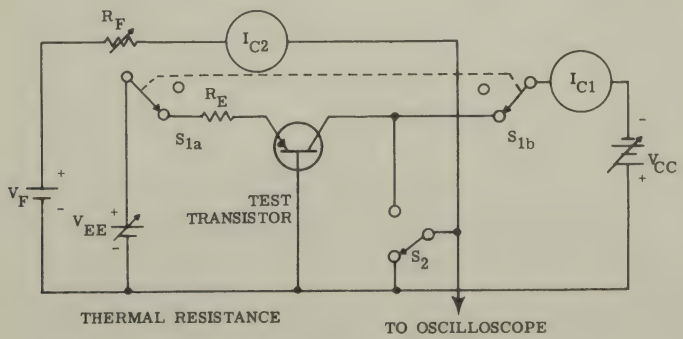


Figure 8-8 — Thermal Resistance Test Circuit

characteristic, such as I_{CBO} or diode voltage, is quickly measured. The temperature-sensitive characteristic must be repeatable and previously calibrated in terms of junction temperature for the particular device. The test circuit in Figure 8-1 can be used to determine I_{CBO} at various temperatures. Thus a certain reading of the characteristic will be associated with a definite junction temperature. Thermal resistance is determined from the equation

$$\theta_{JC} = (T_J - T_C)/P.$$

Collector cutoff current at low voltages and forward diode voltage at low currents are both repeatable characteristics. The circuit of Figure 8-8 uses the collector diode voltage. Power is dissipated when switch S_1 is in the position shown. The switch is then quickly opened and within a short time as compared with the transistor thermal time constant (usually a few milliseconds), switch S_2 is reversed by a mercury relay, and a constant current is injected through the diode. The voltage drop is measured on a scope. A chart of forward voltage versus temperature is consulted, or the scope or a voltmeter can be calibrated directly in thermal resistance.

REFERENCES

IRE standards on methods of testing transistors, IRE Proc. Nov. 1956, Pg. 1543-1560.
R. F. Gates, R. A. Johnson, *"The Measurement of Thermal Resistance"* Syracuse University Research Institute Report EE 542-588R2, Aug. 1, 1958

CHAPTER IX

Transistor Specifications

9-1 — Selection Charts

Motorola Power transistors range from the 2N176 3-ampere 30-volt auto radio devices specified at 2 watts output to the 2N1167 25-ampere 100-volt transistor designed for D-C to D-C converter use and capable of switching 2.5 kilowatts. Power transistors are frequently categorized by current gain, and breakdown voltage to form families of similar types. Motorola power transistors are listed in the handy cross reference charts that follow.

Once a transistor is picked from the reference chart, the data sheet must be consulted to obtain detailed information.

TABLE 9-1

3-AMPERE SERIES TO-3 DIAMOND PACKAGE	BV_{CBO}	h_{FE} @ 0.7A,2V 20 - 60	25 - 90	35 - 120	BV_{CES}
	50	2N350A	2N351A	2N376A	40
	40	2N176*	2N176*	2N669*	30

* *Typical Gain*

TABLE 9-2

3-AMPERE INDUSTRIAL SERIES TO-3 DIAMOND PACKAGE	BV_{CBO}	h_{FE} @ 1A, 2V 35 - 90	60 - 140	BV_{CES}
	120	2N1364	2N1365	100
	100	2N1362	2N1363	75
	80	2N375	2N618	60
	50	2N1359	2N1360	40

TABLE 9-3

5-AMPERE INDUSTRIAL SERIES TO-3 DIAMOND PACKAGE	BV_{CBO}	h_{FE} @ 3A, 2V 20 - 40	35 - 70	50 - 100	75 - 150	BV_{CES}
	120	2N1533	2N1538	2N1543	2N1548	90
	100	2N1532	2N1537	2N1542	2N1547	75
	80	2N1531	2N1536	2N1541	2N1546	60
	60	2N1530	2N1535	2N1540	2N1545	45
	40	2N1529	2N1534	2N1539	2N1544	30

TABLE 9-4

10- AND 15-AMPERE INDUSTRIAL SERIES TO-3 DIAMOND PACKAGE	BV_{CBO}	h_{FE} @ 10A, 2V 10 - 30	30 - 60	50 - 100	BV_{CES}
	100	2N630 2N1552	2N1556	2N1560	75
	80	2N629 2N1551	2N1555	2N1559	60
	60	2N628 2N1550	2N1554	2N1558	45
	40	2N627 2N1549	2N1553	2N1557	30

TABLE 9-5

25-AMPERE INDUSTRIAL SERIES TO-3 DIAMOND PACKAGE	BV_{CBO}	h_{FE} @ 25A, 2V 15 - 65 Pin Types	15 - 65 Lug Types	BV_{CES}
	100	2N1166	2N1167	75
	80	2N1164	2N1165	60
	50	2N1162	2N1163	35

TABLE 9-6

15-AMPERE SERIES TO-36 LOW SILHOUETTE PACKAGE	BV_{CBO}	h_{FE} @ 5A, 2V 20 - 40	25 - 50	35 - 70	BV_{CES}
	100		2N1100	2N1099	80
	80		2N174 2N1358		70
	60	2N443		2N173	50
	50	2N442		2N278	45
	40	2N441		2N277	40

9-2 — Typical Data Sheet Information

Data sheets provide the following types of information:

1. **TYPE OF TRANSISTOR** — type number; method of construction — alloy, diffusion, etc.; PNP or NPN; silicon or germanium.
2. **APPLICATIONS** — switching, amplification, etc.
3. **IMPORTANT FEATURES** — high gain at high current ratings, narrow gain spreads, etc.
4. **OUTLINE DRAWING** — with all dimensions and tolerances, connection to case, availability of pins or solder lugs, etc.
5. **ABSOLUTE MAXIMUM RATINGS** — electrical and thermal limits. The transistor must not be used beyond these absolute limits or permanent damage may occur. The ratings are related to each other and the reader is urged to study Chapter 2 for a complete understanding. The first subscript of the symbol in a PNP transistor indicates the terminal at negative potential. The second subscript is the common circuit terminal. The third subscript indicates the condition of the third terminal with respect to the common terminal.

Example: BV_{CEX} is 100 Vdc (2N1532). Meaning — breakdown voltage will occur when the potential across the collector and emitter terminals is 100 volts or more. The collector is at a negative potential with respect to the emitter, which is the common circuit terminal. "X" indicates that the base terminal has a positive voltage with respect to the emitter, usually much greater than the $I_{CBO} \times R_{BB}$ product.

COMMON VOLTAGE RATINGS

BV_{CEX} — Base-emitter back biased. This is the absolute maximum surge voltage limit.

BV_{CES} — Base-emitter shorted externally. A practical switching limit. This rating is always less than the BV_{CEX} rating and is always tested at a higher current.

BV_{CEO} — Base lead externally open. Practical audio or regulator limit. Generally about 2/3 the value of BV_{CES}, but approaches BV_{CES} at high currents.

BV_{CBO} — Emitter lead externally open. This is the collector diode limit and is generally the same as BV_{CEX}.

BV_{EBO} — Collector lead externally open. This is the emitter diode limit.

COMMON CURRENT RATINGS

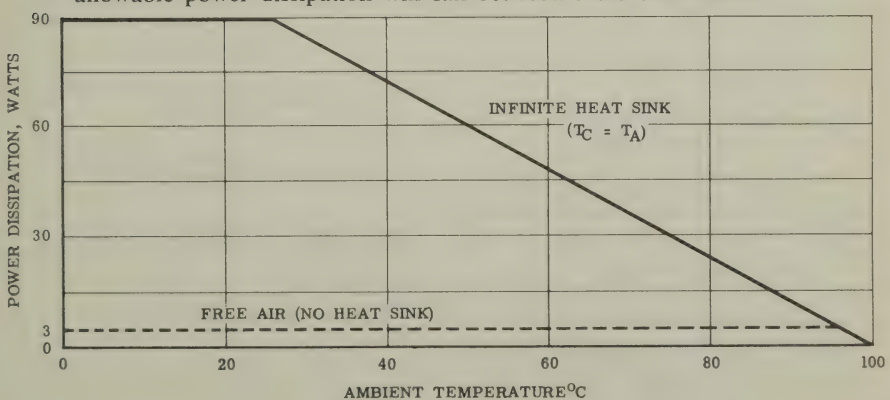
Collector Current (Continuous) — The limit for maximum reliable operation (see Chapter 2).

Collector Current (Peak) — This is the limit based on safe breakdown (see Chapter 2).

6. **TEMPERATURE-POWER RATINGS**

Collector Junction Temperature — A true limit. Power dissipation and thermal resistance, each of which are related to temperature rise, are listed here for convenient reference (see Chapter 2).

Temperature Derating Curve — This is a typical curve, applicable to all Motorola Industrial Power Transistors having a maximum power rating of 90 watts. With an infinite heat sink, case temperature equals the ambient temperature. In free air, with no heat sink, case temperature is only slightly lower than the maximum junction temperature of 100°C, and the allowable power dissipation is appreciably less. With a typical heat sink, allowable power dissipation will fall between these two curves.



7. ELECTRICAL CHARACTERISTICS

I_{CBO} is tested for a maximum value at approximately two-thirds of BV_{CBO} and at 2 volts. These low-temperature tests are made at 25°C case temperature. A high-temperature rating is also necessary and is made at one-half of BV_{CES} and at 90°C.

I_{EBO} is an indication of back-bias current flow.

BV_{CES}, BV_{CEX}, BV_{CEO}, and BV_{CBO} are ensured by testing to the characteristic test points given.

Current Gain values fall within the two-to-one range given. This is the ratio of I_C/I_B.

Base-Emitter Drive Voltage is the voltage necessary to maintain saturation at the values given for I_B and I_C.

Collector Saturation Voltage is a measure of the efficiency of a transistor when it is switched fully on and tested at a forced current gain of 10.

Frequency Cutoff is usually specified for the common-emitter configuration and is rather low for most power devices. Feedback may be used to increase the circuit cutoff frequency.

Switching Characteristics are associated with a specific circuit shown on the data sheet, or the ON base current, I_{B1}, and OFF base current, I_{B2}, are specified.

Transconductance, I_C/V_{BE}, is an indication of the base voltage required to obtain a specified collector current when the transistor is out of saturation.

8. CHARACTERISTIC CURVES

Typical curves which show relationships of current, voltage, gain and temperature, enabling the designer to select proper operating points for his application.

9-3—Abbreviations and Symbols

The following are abbreviations generally used by industry.

Symbol	Meaning	Symbol	Meaning
A	Ampere (ac rms or dc)	BV_{CES}	Breakdown voltage, collector-to-emitter junction reverse biased (base shorted)
a	Ampere (peak)	BV_{CEX}	Breakdown voltage, collector-to-emitter junction reverse biased (base-emitter back biased)
B	Base electrode	C	Capacitance and collector electrode
BV	Breakdown voltage	C_c	Internal collector junction capacitance
BV_{CBO}	Breakdown voltage, collector-to-base junction reverse biased (emitter open)	C (dep)	Depletion layer capacitance
BV_{CEO}	Breakdown voltage, collector-to-emitter junction reverse biased (base open)	C (dif)	Diffusion capacitance
BV_{CER}	Breakdown voltage, collector-to-emitter junction reverse biased (specified resistance)	C_{ib}	Input capacitance, common base

Symbol	Meaning
C_L	Load capacitance
C_{ob}	Output capacitance, common base
C_{oe}	Output capacitance, common emitter
ΔV_Z	Zener voltage regulation
E	Emitter electrode
f	Frequency
f_{ab}	Common base small-signal short-circuit forward current transfer-ratio cutoff frequency (emitter input)
f_{ae}	Common emitter small-signal short-circuit forward current transfer-ratio cutoff frequency
f_{ref}	Reference frequency
f_{osc}	Maximum frequency of oscillation
f_{pg}	Power gain cutoff frequency
f_τ	Frequency at which common emitter current gain is unity
G_b	Power gain (common base)
G_c	Power gain (common collector)
G_e	Power gain (common emitter)
g_M, g_{FE}	Static or D-C transconductance
g_m	Small-signal transconductance
G_M, G_{FE}	Large-signal transconductance

Symbol	Meaning
h_{fb}	Common base small-signal short-circuit forward current transfer-ratio
h_{fe}	Common emitter small-signal short-circuit forward current transfer-ratio (base input)
h_{FE}	Common-emitter DC short-circuit forward current transfer-ratio current gain I_C/I_B
H_{FE}	Common emitter large-signal short-circuit forward current transfer-ratio
h_{ib}	Common base small-signal short-circuit input impedance (emitter input)
h_{ie}	Common emitter small-signal short-circuit input impedance (base input)
h_{ob}	Common base small-signal open-circuit output admittance (emitter input)
h_{oc}	Common collector small-signal open-circuit output admittance (base input)
h_{oe}	Common emitter small-signal open-circuit output admittance (base input)
h_{rb}	Common base small-signal open-circuit reverse-transfer voltage ratio (emitter input)
h_{rc}	Common collector small-signal open-circuit reverse-transfer voltage ratio (base input)
h_{re}	Common emitter small-signal open-circuit reverse-transfer voltage ratio (base input)
I	Current
$i_{(surge)}$	Surge current
I_B	Average base current (dc)
I_b	Instantaneous base current (ac rms)
i_b	Base current (peak)

Symbol	Meaning
I_C	Collector current (dc)
I_c	Collector current (ac rms)
i_c	Collector current (peak)
I_{CBO}, I_{CO}	Collector cutoff current (emitter open)
I_{CEO}	Collector cutoff current (base open)
I_{CER}	Collector cutoff current (specified resistor from base to emitter)
I_{CERV}	Collector cutoff current (reverse voltage on base)
I_{CES}	Collector cutoff current (base shorted to emitter)
I_E	Average emitter current (dc)
I_e	Instantaneous emitter current (ac rms)
i_e	Instantaneous emitter current (peak)
I_{EBO}	Emitter cutoff current (collector open)
I_F	Forward current (dc)
i_F	Forward current (peak)
i_{Fr}	Forward recovery current (specified instantaneous value)
I_o	Output current (dc)
I_R	Reverse current (dc)
i_R	Reverse current (peak)
i_{Rr}	Reverse recovery current (specified instantaneous value)
I_Z	Average Zener current
I_{ZK}	Zener knee current
I_{ZM}	Zener maximum current
I_{ZT}	Zener test current
i_z	Instantaneous zener current (ac rms)
K	Kilohm
kc	Kilocycles per second
L_c	Conversion loss
m	Thousandth
mA	Milliampere (average)
ma	Milliampere (peak)
mAac	Milliampere (ac rms)
mAdc	Milliampere (dc)
mc	Megacycles per second
μ	Micro (millionth)
μA	Microampere (average)
μa	Microampere (peak)

Symbol	Meaning
μf	Microfarad
μh	Microhenry
μmho	Micromho
mW	Milliwatt (max, average, or rms)
mw	Milliwatt (peak)
NF	Noise figure
nsec	Millimicrosecond (nano)
Ω	Ohms
P	Power dissipation of all terminals (average total)
p	Power dissipation all terminals (peak)
P_b	Power dissipation of base (average)
p_b	Power dissipation of base (peak)
P_c	Power dissipation of collector (average)
p_c	Power dissipation of collector (peak)
P_d	Power dissipation of device
P_e	Power dissipation of emitter (average)
p_e	Power dissipation of emitter (peak)
pf	Micro microfarad (pico)
PIV	Peak inverse voltage
Q	Transistor
r'_b, r_{BB}'	Internal base spreading resistance
R_B	External base resistance
R_C	External collector resistance
R_E	External emitter resistance
$R_{(sat)}$	Saturation resistance
R_L	Resistance, load
rms	Root mean square
T	Temperature
t	Time
T_A	Temperature, ambient
T_C	Temperature, case
TCBV	Temperature coefficient of breakdown voltage
t_d	Pulse delay time
t_f	Pulse fall time
t_{fr}	Forward recovery time
T_J	Temperature junction

Symbol	Meaning
t_P	Pulse time
t_r	Pulse rise time
t_s	Pulse storage time
θ_{CA}	Thermal resistance, case to ambient
θ_{JA}	Thermal resistance, junction to air
θ_{JC}	Thermal resistance, junction to case
V	Volt (dc)
v	Volt (peak)
Vac	Volt (ac rms)
V_{BB}	Base voltage (dc) supply
V_{BE}	Emitter voltage (dc) (base to emitter)
V_{CC}	Collector voltage (dc) supply
$V_{CE(sat)}$	Collector to emitter saturation voltage
V_{EC}	Emitter voltage (dc) (emitter to collector)
V_{EE}	Emitter voltage (dc) supply
V_{fe}	Floating potential
V_F	Forward voltage drop
V_O	Output voltage (dc)
v_o	Output voltage (ac)
V_{PT}	Voltage, punch-through
V_R	Reverse voltage (dc)
V_r	Reverse voltage (peak)
V_Z	Zener voltage
W	Watts (max, ave, rms)
w	Watts (peak)
Z_z	Zener impedance
Z_{zk}	Zener impedance, knee
Z_{zt}	Zener impedance, test
ρ	Resistivity
η	Efficiency
∂	Partial derivative
ϕ	Flux
τ	Time constant
ϵ	Natural logarithm

9-4—Specifications

(Case Drawings and Derating Curves on Pages 200 to 205)

2N375, 2N618, 2N1359, 2N1360, 2N1362, 2N1363, 2N1364, 2N1365 (See Case No. 1 – Derating Curve No. 1)

Motorola types 2N1359-60, 2N375, 2N618, and 2N1362-65 are germanium PNP high voltage power transistors designed to use in high quality industrial and military equipment. All units are specified to include close parameter control for switching and amplifier applications throughout the audio frequency range. The hermetically sealed, industry standard TO-3 package, originally developed by Motorola, is designed to meet or exceed the mechanical and environmental requirements of military specification MIL-S-19500.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	2N1359 2N1360	2N375 2N618	2N1362 2N1363	2N1364 2N1365	Unit
Collector to Base Voltage	BV_{CBO}	50	80	100	120	Vdc
Collector to Emitter Voltage	BV_{CES}	40	60	75	100	Vdc
Collector Current (continuous)	I_C	3	3	3	3	amp
Collector Current (Peak)	I_C	10	10	10	10	amp
Collector Dissipation, 25°C Mounting Base Temperature	P_C	90	90	90	90	watt
Collector Junction Temperature	T_J	100	100	100	100	°C

ELECTRICAL CHARACTERISTICS, GENERAL (at 25°C Mounting Base Temperature)

Characteristic	Symbol	Min	Max	Unit
Collector-Base Cutoff Current	I_{CBO}			
$V_{CB} = 40V$ (2N1359, 2N1360)		—	3.0	mA
$V_{CB} = 60V$ (2N375, 2N618)		—	3.0	mA
$V_{CB} = 75V$ (2N1362, 2N1363)		—	3.0	mA
$V_{CB} = 100V$ (2N1364, 2N1365)		—	3.0	mA
Collector-Base Cutoff Current at $T_B = +90°C$, $V_{CB} = ½\ BV_{CES}$ Rating	I_{CBO}	—	20	mA
Emitter-Base Cutoff Current $V_{EB} = 12V$	I_{EBO}	—	0.5	mA
Collector-Emitter Breakdown Voltage $I_C = 500$ ma, $V_{EB} = 0$	BV_{CES}			
2N1359, 2N1360		40	—	Vdc
2N375, 2N618		60	—	Vdc
2N1362, 2N1363		75	—	Vdc
2N1364, 2N1365		100	—	Vdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Thermal Resistance Junction to Case	θ_{JC}	—	0.6	0.8	°C/W
Thermal Time Constant		—	50	—	millisec

ELECTRICAL CHARACTERISTICS, COMMON EMITTER (at 25°C Mounting Base Temperature)

Characteristic	Symbol	2N1359, 2N375, 2N1362, 2N1364			2N1360, 2N618, 2N1363, 2N1365			Unit
		Min	Typ	Max	Min	Typ	Max	
Current Gain	h_{FE}							
$V_{CE} = 4V, I_C = 1.0A$		35	55	90	60	90	140	
$V_{CE} = 4V, I_C = 3.0A$		15	22	—	20	35	—	
Transconductance	g_{FE}							
$V_{CE} = 4V, I_C = 1.0A$		0.8	1.25	—	1.0	1.6	—	mhos
Frequency Cutoff	$f_{\alpha e}$							
$V_{CE} = 4V, I_C = 1.0A$		7	10	—	5	8.5	—	kc
Collector Saturation Voltage	$V_{CE(SAT)}$							
$I_C = 2.0A, I_B = 200$ mA		—	0.4	1.0	—	0.3	0.8	Vdc
Base-Emitter Drive Voltage	V_{BE}							
$I_C = 2.0A, I_B = 200$ mA		—	0.7	—	—	0.6	—	Vdc

SWITCHING CHARACTERISTICS, TYPICAL

Saturated Collector Current	Pulsed Drive Base Current		Response Time in μsec		
	On	Off	T_R	T_S	T_F
	300 ma		10		
3A		100 ma		5	20

2N627, 2N628, 2N629, 2N630 (See Case No. 2 , 3 – Derating Curve No. 1)

Motorola types 2N627 through 2N630 are germanium PNP alloy-junction power transistors with collector common to case. They are designed for high-current switching and audio applications. High current gain at 10 amperes, conservative maximum collector to base voltage ratings, low saturation resistance, thermal resistance below 0.8°C/W and built-in voltage transient protection allows efficient and reliable use in switching applications. Ring emitter internal design and hermetically sealed standard TO-3 package with solder terminals* meets or exceeds the mechanical and environmental requirements of military specification MIL-S-19500.

*Units are also available without solder terminals as types MN-61A through MN-64A. These units have .052" dameter X .360" long pins.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	2N627 (MN-61A)	2N628 (MN-62A)	2N629 (MN-63A)	2N630 (MN-64A)	Unit
Collector to Base Voltage	BV_{CBO}	40	60	80	100	Vdc
Collector to Emitter Voltage	BV_{CES}	30	45	60	75	Vdc
Emitter to Base Voltage	BV_{EBO}	20	30	40	50	Vdc
Collector Current (based on maximum at which characteristics are specified. Permanent damage will not result if this rating and no other is exceeded.)	I_C	10	10	10	10	amp
Maximum Junction Temperature — Continuous	T_J	100	100	100	100	°C
Collector Dissipation for Mounting Base Temperature of 25°C (See Power-Temperature Derating Curve)	P_C	90	90	90	90	watt

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance Junction to Case	θ_{JC}	0.6	0.8	°C/W

ELECTRICAL CHARACTERISTICS, GENERAL

at mounting base-temperature 25°C ± 3°C except where noted

Characteristic	Symbol	Min	Typ	Max	Unit
Collector Cutoff Current $V_{CB} = BV_{CBO}$(max), $I_E = 0$ (all types)	I_{CBO}	—	4	20	mAdc
Collector Cutoff Current $V_{CB} = 2V$, $I_E = 0$ (all types)	I_{CBO}	—	100	200	μAdc
Collector Cutoff Current $V_{CB} = 15V$, $I_E = 0$, $T_A = 90°C$ 2N267,28 2N629,30	I_{CBO}	— —	10 —	20 —	mAdc
Collector Cutoff Current $V_{CB} = 30V$, $I_E = 0$, $T_A = 90°C$ 2N627,28 2N629,30	I_{CBO}	— —	— 10	— 20	mAdc
Emitter Cutoff Current $V_{EB} = 12V$, $I_C = 0$ (all types)	I_{EBO}	—	0.4	1.0	mAdc
Collector to Emitter Saturation Voltage $I_C = 10A$, $I_B = 1A$ (all types)	$V_{CE(SAT)}$	—	0.4	1.0	Vdc
Base to Emitter Drive Voltage $I_C = 10A$, $I_B = 1A$ (all types)	V_{EB}	—	0.7	—	Vdc
Collector-Emitter Breakdown Voltage $I_C = 250$ ma, $V_{EB} = 0$ 2N627 2N628 2N629 2N630	BV_{CES}	30 45 60 75	— — — —	— — — —	volts

ELECTRICAL CHARACTERISTICS, COMMON EMITTER

Characteristic	Symbol	Min	Typ	Max	Unit
DC Forward Current Gain $V_{CE} = 2V$, $I_C = 1.0A$ $V_{CE} = 2V$, $I_C = 10.0A$	h_{FE}	— 10	— —	175 30	
DC Forward Transconductance $V_{CE} = 2V$, $I_C = 10.0A$	g_{FE}	6	12	18	mho
Current Gain Frequency Cutoff, Small Signal $V_{CE} = 2V$, $I_C = 2A$	$f_{\alpha e}$	5	8	—	kc
Power Gain Power Output = 2 watts, f = 1kc $R_L = 26\Omega$, $V_{CE} = 12V$, $R_S = 10\Omega$, $I_C = 0.5A$	G_e	—	38	—	db
Small Signal Current Gain f = 1kc, $V_{CE} = 12V$, $I_C = 0.5A$	h_{fe}	—	60	—	
Small Signal Input Impedance f = 1kc, $V_{CE} = 12V$, $I_C = 0.5A$	h_{ie}	—	15	—	ohm

2N1162, 2N1163, 2N1164, 2N1165, 2N1166, 2N1167

(See Case No. 2, 3 – Derating Curve No. 1)

Motorola types 2N1162 through 2N1167 are germanium PNP, alloy-junction power transistors with collector common to case. They are designed for high current switching and audio applications. High current gain at 25 amperes, conservative maximum voltage ratings and low saturation resistance allows efficient and reliable use in switching applications. Rugged internal design and hermetically sealed standard TO-3 package with or without solder terminals* meets or exceeds the mechanical and environmental requirements of military specification MIL-T-19500A.

*The 2N1162, 2N1164, and 2N1166 are supplied with .052" pins. The 2N1163, 2N1165 and 2N1167 have solder lugs attached.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	2N1162 2N1163	2N1164 2N1165	2N1167 2N1166	Unit
Collector to Base Voltage	BV_{CBO}	50	80	100	volts
*Collector to Emitter Voltage	BV_{CES}	35	60	75	volts
Collector DC Current	I_C	25	25	25	amps
Junction Temperature — Continuous (2)		90	90	90	°C
Junction Temperature — Intermittent (2)		100	100	100	°C
Collector Dissipation, Mounting Base Temperature of 30°C		50	50	50	watts

*BV_{CES} test swept to 1.0 ampere to assure reliable operation.

SWITCHING CHARACTERISTICS, TYPICAL

Saturated Collector Current	Pulsed Drive Base Current		Response Times in μ sec		
	On	Off	Td + Tr	T_S	T_F
5 amps	330 ma		11		
		100 ma		5	17
10 amps	660 ma		15		
		200 ma		4	20
25 amps	1700 ma		19		
		500 ma		3	18

THERMAL CHARACTERISTICS, MAXIMUM

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Mounting Case	θ_{JC}	1.2	°C/Watt

ELECTRICAL CHARACTERISTICS, COMMON EMITTER

Characteristic	Symbol	Min	Typ	Max	Unit
DC Forward Current Gain	h_{FE}				
$V_{CE} = 2V, I_C = 5A$		—	65	125	—
$V_{CE} = 1V, I_C = 25A$		15	25	65	—
Current Gain Frequency Cutoff, Small Signal	f_{ae}				
$V_{CE} = 2V, I_C = 2A$		—	4	—	kc

ELECTRICAL CHARACTERISTICS, GENERAL*

Characteristic	Symbol	Min	Typ	Max	Unit
Collector Cutoff Current	I_{CBO}				
$V_{CB} = BV_{CBO}$ (max), $I_E = 0$		—	3	15	ma
$V_{CB} = 2V$, $I_E = 0$		—	125	225	μa
$V_{CB} = 15V$, $I_E = 0$, $T_A = 90°C$ (2N1162, 2N1163)		—	10	20	ma
$V_{CB} = 30V$, $I_E = 0$, $T_A = 90°C$ (2N1164 thru 2N1167)		—	10	20	ma
Emitter Cutoff Current	I_{EBO}				
$V_{EB} = 12V$, $I_C = 0$		—	0.5	1.2	ma
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$				
$I_C = 25A$, $I_B = 1.6A$		—	0.3	1.0	volts
Base to Emitter Drive Voltage, (at Saturation)	V_{EB}				
$I_C = 25A$, $I_B = 1.6A$		—	0.7	—	volts

*At base temperature of 25°C ± 3°C except where noted.

2N1529 thru 2N1538 (See Case No. 1 – Derating Curve No. 1)

Motorola types 2N1529 through 2N1538 are germanium PNP alloy power transistors designed for use in high-quality industrial and military applications. Close parameter control provides reliable design in switching and amplifier applications from DC through the audio frequency range. High voltage and current ratings allow operation as a switch at power levels up to 500 watts. The hermetically sealed, industry standard TO-3 package, originally developed by Motorola, is designed to meet the mechanical and environmental requirements of military specification MIL-T-19500.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	2N1529 2N1534	2N1530 2N1535	2N1531 2N1536	2N1532 2N1537	2N1533 2N1538	Unit
Collector to Emitter Voltage	BV_{CEX}	40	60	80	100	120	Vdc
Collector to Emitter Voltage	BV_{CES}	30	45	60	75	90	Vdc
Collector to Emitter Voltage	BV_{CEO}	20	30	40	50	60	Vdc
Collector to Base Voltage	BV_{CBO}	40	60	80	100	120	Vdc
Emitter to Base Voltage	BV_{EBO}	20	30	40	50	60	Vdc
Collector Current (Continuous)	I_C	5	5	5	5	5	amp
Collector Current (Peak)	I_C	10	10	10	10	10	amp
Collector Junction Temperature	T_J	100	100	100	100	100	°C
Collector Dissipation (25°C Mtg. Base Temp.)	P_C	90	90	90	90	90	watt

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typical	Maximum	Unit
Thermal Resistance	θ_{JC}	0.6	0.8	°C/W

ELECTRICAL CHARACTERISTICS, GENERAL (At 25°C Mounting Base Temperature)

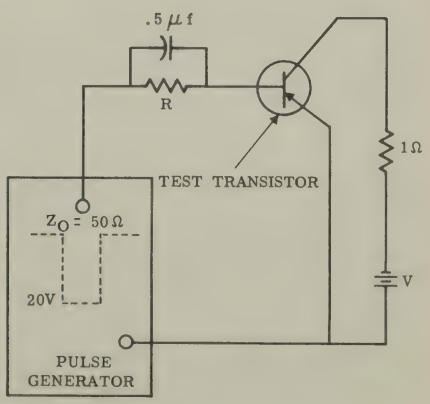
Parameter	Symbol	Min	Typ	Max	Unit
Collector-Base Cutoff Current	I_{CBO}				
$V_{CB} = -25V$ 2N1529—2N1538		—	—	2.0	mA
$V_{CB} = -40V$		—	—	2.0	mA
$V_{CB} = -55V$		—	—	2.0	mA
$V_{CB} = -65V$		—	—	2.0	mA
$V_{CB} = -80V$		—	—	2.0	mA
Collector-Base Cutoff Current	I_{CBO}				
$V_{CB} = -2V$ (all types)		—	—	200	μA
Collector-Base Cutoff Current at $T_B = +90°C$	I_{CBO}				
$V_{CB} = ½ BV_{CES}$ rating		—	—	20	mA
Emitter-Base Cutoff Current	I_{EBO}				
$V_{EB} = 12V$ (all types)		—	—	0.5	mA
Collector-Emitter Breakdown Voltage	BV_{CES}				
$I_C = 500mA$, $V_{EB} = 0$					
2N1529—2N1538		30	—	—	volts
		45	—	—	volts
		60	—	—	volts
		75	—	—	volts
		90	—	—	volts
Collector-Emitter Leakage Current	I_{CEX}				
$V_{BE} = 1.0V$					
$V_{CE} = 40$ 2N1529—2N1538		—	—	20	mA
$V_{CE} = 60$		—	—	20	mA
$V_{CE} = 80$		—	—	20	mA
$V_{CE} = 100$		—	—	20	mA
$V_{CE} = 120$		—	—	20	mA
Collector-Emitter Breakdown Voltage	BV_{CEO}				
$I_C = 500mA$, $I_B = 0$					
2N1529—2N1538		20	—	—	volts
		30	—	—	volts
		40	—	—	volts
		50	—	—	volts
		60	—	—	volts
Collector-Base Breakdown Voltage	BV_{CBO}				
$I_C = 20mA$					
2N1529—2N1538		40	—	—	volts
		60	—	—	volts
		80	—	—	volts
		100	—	—	volts
		120	—	—	volts

ELECTRICAL CHARACTERISTICS, COMMON EMITTER (At 25°C Mounting Base Temperature)

Characteristics	Symbol	Min	Typ	Max	Unit
Current Gain	h_{FE}				
$V_{CE} = -2V, I_C = 3A$					
2N1529—2N1538		20	—	40	—
		35	—	70	—
Base-Emitter Drive Voltage	V_{BE}				
$I_C = 3A, I_B = 300mA$					
2N1529—2N1538		—	—	1.7	volts
		—	—	1.5	volts
Collector Saturation Voltage	$V_{CE(SAT)}$				
$I_C = 3A, I_B = 300mA$					
2N1529—2N1538		—	0.6	1.5	volts
		—	0.4	1.2	volts
Frequency Cutoff	$f_{\alpha e}$				
$V_{CE} = -2V, I_C = 3A$					
2N1529—2N1538		—	10	—	kc
		—	8.5	—	kc
Switching Characteristics					
$I_C = 3A$					
Delay + Rise Time	$t_d + t_r$	—	10	—	μsec
2N1529—2N1538		—	8	—	μsec
Storage Time	t_s	—	2	—	μsec
2N1529—2N1538		—	3	—	μsec
Fall Time	t_f	—	5	—	μsec
2N1529—2N1538		—	5	—	μsec
Transconductance	g_{FE}				
$V_{CE} = -2V, I_C = 3A$					
2N1529—2N1538		1.2	2.0	—	mhos
		1.5	2.5	—	mhos

SWITCHING TIME MEASURING UNIT

	2N1529-33	2N1534-38
I_C (Amps)	3	3
V (Volts)	3	3
I_{ON} (ma)	300	200
R ohms	65	100
$t_d + t_r$ (μsec)	10	8
t_s (μsec)	2	3
t_f (μsec)	5	5



2N1539 thru 2N1548 (See Case No. 3 – See Derating Curve No. 1)

Motorola types 2N1539 thru 2N1548 are germanium PNP alloy power transistors designed for use in high-quality industrial and military applications. Close parameter control provides reliable design in switching and amplifier applications from DC through the audio frequency range. High transconductance and low saturation resistance make these types extremely useful for efficient converter applications, and high voltage and current ratings allow operation as a switch at power levels up to 500 Watts. The hermetically sealed, industry standard TO-3 package, originally developed by Motorola, is designed to meet the mechanical and environmental requirements of military specification MIL-S-19500.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	2N1539 2N1544	2N1540 2N1545	2N1541 2N1546	2N1542 2N1547	2N1543 2N1548	Unit
Collector to Emitter Voltage	BV_{CEX}	40	60	80	100	120	Vdc
Collector to Emitter Voltage	BV_{CES}	30	45	60	75	90	Vdc
Collector to Emitter Voltage	BV_{CEO}	20	30	40	50	60	Vdc
Collector to Base Voltage	BV_{CBO}	40	60	80	100	120	Vdc
Emitter to Base Voltage	BV_{EBO}	20	30	40	50	60	Vdc
Collector Current (Continuous)	I_C	5	5	5	5	5	amp
Collector Current (Peak)	I_C	10	10	10	10	10	amp
Collector Junction Temperature	T_j	100	100	100	100	100	°C
Collector Dissipation (25°C Mtg. Base Temp.)	P_C	90	90	90	90	90	watt

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typical	Maximum	Unit
Thermal Resistance	θ_{JC}	0.6	0.8	°C/W

ELECTRICAL CHARACTERISTICS, GENERAL (At 25°C Mounting Base Temperature)

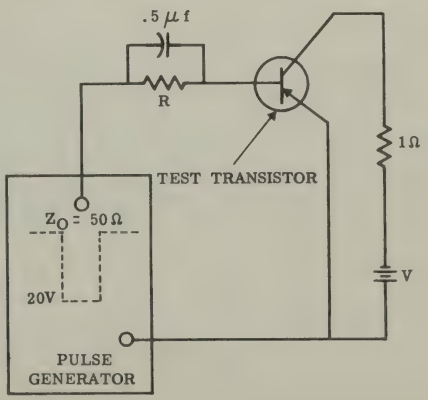
Parameter	Symbol	Min	Typ	Max	Unit
Collector-Base Cutoff Current	I_{CBO}				
$V_{CB} = -25V$ 2N1539—2N1548		—	—	2.0	mA
$V_{CB} = -40V$		—	—	2.0	mA
$V_{CB} = -55V$		—	—	2.0	mA
$V_{CB} = -65V$		—	—	2.0	mA
$V_{CB} = -80V$		—	—	2.0	mA

ELECTRICAL CHARACTERISTICS, GENERAL *(continued)*

Parameter	Symbol	Min	Typ	Max	Unit
Collector-Base Cutoff Current	I_{CBO}				
$V_{CB} = -2V$ (all types)		—	—	200	μA
Collector-Base Cutoff Current at $T_B = +90°C$	I_{CBO}				
$V_{CB} = ½ BV_{CES}$ rating		—	—	20	mA
Emitter-Base Cutoff Current	I_{EBO}				
$V_{EB} = 12V$ (all types)		—	—	0.5	mA
Collector-Emitter Breakdown Voltage	BV_{CES}				
$I_C = 500mA$, $V_{EB} = 0$					
2N1539		30	—	—	volts
2N1540		45	—	—	volts
2N1541		60	—	—	volts
2N1542		75	—	—	volts
2N1543		90	—	—	volts
Collector-Emitter Leakage Current	I_{CEX}				
$V_{BE} = 1.0V$					
$V_{CE} = 40$ 2N1539—2N1548		—	—	20	mA
$V_{CE} = 60$		—	—	20	mA
$V_{CE} = 80$		—	—	20	mA
$V_{CE} = 100$		—	—	20	mA
$V_{CE} = 120$		—	—	20	mA
Collector-Emitter Breakdown Voltage	BV_{CEO}				
$I_C = 500mA$, $I_B = 0$					
2N1539		20	—	—	volts
2N1540		30	—	—	volts
2N1541		40	—	—	volts
2N1542		50	—	—	volts
2N1543		60	—	—	volts
Collector-Base Breakdown Voltage	BV_{CBO}				
$I_C = 20mA$					
2N1539		40	—	—	volts
2N1540		60	—	—	volts
2N1541		80	—	—	volts
2N1542		100	—	—	volts
2N1543		120	—	—	volts

SWITCHING TIME MEASURING UNIT

	2N1539-43	2N1544-48
I_C (Amps)	3	3
V (Volts)	3	3
I_{ON} (ma)	120	80
R (ohms)	165	250
$t_d + t_r$ (μsec)	5	5
t_s (μsec)	3	3
t_f (μsec)	5	8



ELECTRICAL CHARACTERISTICS, COMMON EMITTER (At 25°C Mounting Base Temperature)

Characteristics	Symbol	Min	Typ	Max	Unit
Current Gain	h_{FE}				
$V_{CE} = -2V, I_C = 3A$					
2N1539—2N1548		50	—	100	—
		75	—	150	—
Base-Emitter Drive Voltage	V_{BE}				
$I_C = 3A, I_B = 300mA$					
2N1539—2N1548		—	—	0.7	volts
		—	—	0.5	volts
Collector Saturation Voltage	$V_{CE(SAT)}$				
$I_C = 3A, I_B = 300mA$					
2N1539—2N1548		—	0.2	0.6	volts
		—	0.1	0.3	volts
Frequency Cutoff	$f_{\alpha e}$				
$V_{CE} = -2V, I_C = 3A$					
2N1539—2N1548		—	4	—	kc
		—	4	—	kc
Switching Characteristics					
$I_C = 3A$					
Delay + Rise Time	$t_d + t_r$				
2N1539—2N1548		—	5	—	μsec
		—	5	—	μsec
Storage Time	t_s				
2N1539—2N1548		—	3	—	μsec
		—	3	—	μsec
Fall Time	t_f				
2N1539—2N1548		—	5	—	μsec
		—	8	—	μsec
Transconductance	g_{FE}				
$V_{CE} = -2V, I_C = 3A$					
2N1539—2N1548		3.0	6.0	—	mhos
		5.0	7.5	—	mhos

2N1549 thru 2N1552

(See Case No. 2, 3 – See Derating Curve No. 1)

Motorola types 2N1549 thru 2N1552 are germanium PNP alloy-junction power transistors with collector common to case. They are designed for high-current switching and audio applications. Conservative maximum voltage and current rating allow reliable operation at power levels up to 1200 watts. Extremely fast switching speed allows their usage in converters at extended frequencies. Rugged internal design and hermetically sealed standard TO-3 package is designed to meet the mechanical and environmental requirements of military specification MIL-S-19500. For units with solder lugs attached, specify devices MP1549 through MP1552.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	2N1549	2N1550	2N1551	2N1552	Unit
Collector to Emitter Voltage	BV_{CEX}	40	60	80	100	Vdc
Collector to Emitter Voltage	BV_{CES}	30	45	60	75	Vdc
Collector to Emitter Voltage	BV_{CEO}	20	30	40	50	Vdc
Collector to Base Voltage	BV_{CBO}	40	60	80	100	Vdc
Emitter to Base Voltage	BV_{EBO}	20	30	40	50	Vdc
Collector Current (Continuous)	I_C	15	15	15	15	amp
Collector Current (Peak)	I_C	20	20	20	20	amp
Collector Junction Temperature	T_j	100	100	100	100	°C
Collector Dissipation (25°C Mtg. Base Temp.)	P_C	90	90	90	90	watt

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typical	Maximum	Unit
Thermal Resistance	θ_{JC}	0.6	0.8	°C/W

ELECTRICAL CHARACTERISTICS, COMMON EMITTER (At 25°C Mounting Base Temperature)

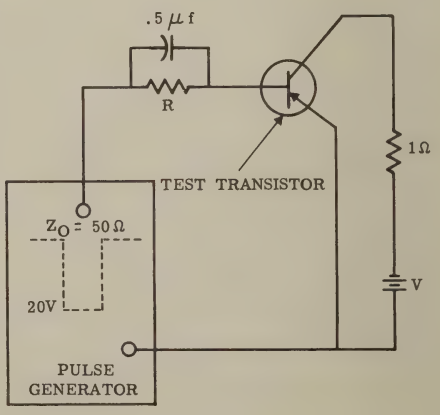
Current Gain	h_{FE}				
$V_{CE} = 2V, I_C = 10A$ (all types)		—	—	30	—
Base-Emitter Drive Voltage	V_{BE}				
$I_C = 10A, I_B = 1.0A$ (all types)		10	—	1.3	volts
Collector Saturation Voltage	$V_{CE(SAT)}$				
$I_C = 10A, I_B = 1.0A$ (all types)		—	0.5	1.0	volts
Transconductance	g_{FE}				
$V_{CE} = 2V, I_C = 10A$ (all types)		6	12	18	mhos
Switching Characteristics					
$I_C = 10A$					
Delay + Rise Time (all types)	$t_d + t_r$	—	5	—	μsec
Storage Time (all types)	t_s	—	2	—	μsec
Fall Time (all types)	t_f	—	10	—	μsec
Frequency Cutoff	f_{ae}				
$V_{CE} = 2V, I_C = 5A$ (all types)		—	10	—	kc

ELECTRICAL CHARACTERISTICS, GENERAL (At 25°C Mounting Base Temperature)

Parameter		Symbol	Min	Typ	Max	Unit
Collector-Base Cutoff Current		I_{CBO}				
$V_{CB} = 25V$	2N1549		—	—	3.0	mA
$V_{CB} = 40V$	2N1550		—	—	3.0	mA
$V_{CB} = 55V$	2N1551		—	—	3.0	mA
$V_{CB} = 65V$	2N1552		—	—	3.0	mA
Collector-Base Cutoff Current		I_{CBO}				
$V_{CB} = 2V$ (all types)			—	—	200	μA
Collector-Base Cutoff Current		I_{CBO}				
at $T_B = +90°C$						
at $V_{CB} = ½ BV_{CES}$ rating			—	—	20	mA
Emitter-Base Cutoff Current		I_{EBO}				
$V_{EB} = 12V$ (all types)			—	—	0.5	mA
Collector-Emitter Breakdown Voltage		BV_{CES}				
$I_C = 300mA, V_{EB} = 0$						
	2N1549		30	—	—	volts
	2N1550		45	—	—	volts
	2N1551		60	—	—	volts
	2N1552		75	—	—	volts
Collector-Emitter Leakage Current		I_{CEX}				
$V_{BE} = 1.0V$						
$V_{CE} = 40$	2N1549		—	—	20	mA
$V_{CE} = 60$	2N1550		—	—	20	mA
$V_{CE} = 80$	2N1551		—	—	20	mA
$V_{CE} = 100$	2N1552		—	—	20	mA
Collector-Emitter Breakdown Voltage		BV_{CEO}				
$I_C = 300mA, I_B = 0$						
	2N1549		20	—	—	volts
	2N1550		30	—	—	volts
	2N1551		40	—	—	volts
	2N1552		50	—	—	volts
Collector-Base Breakdown Voltage		BV_{CBO}				
$I_C = 20mA$						
	2N1549		40	—	—	volts
	2N1550		60	—	—	volts
	2N1551		80	—	—	volts
	2N1552		100	—	—	volts

SWITCHING TIME MEASURING UNIT

	2N1549-52
I_C (Amps)	10
V (Volts)	10
I_{ON} (Amps)	2
R (ohms)	10
$t_d + t_r$ (μsec)	5
t_s (μsec)	2
t_f (μsec)	10



2N1553 thru 2N1560 (See Case No. 2, 3 – Derating Curve No. 1)

Motorola types 2N1553 thru 2N1560 are germanium PNP industrial alloy power transistors with collector common to case. They are characterized by high efficiency and power gain in converter and switching circuits. Conservative maximum voltage and current ratings allow reliable operation as a switch at power levels up to 1200 watts. Rugged internal design and hermetically sealed standard TO-3 package is designed to meet the mechanical and environmental requirements of military specification MIL-S-19500. For units with solder lugs attached, specify devices MP1553 through MP1560.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	2N1553 2N1557	2N1554 2N1558	2N1555 2N1559	2N1556 2N1560	Unit
Collector to Emitter Voltage	BV_{CEX}	40	60	80	100	Vdc
Collector to Emitter Voltage	BV_{CES}	30	45	60	75	Vdc
Collector to Emitter Voltage	BV_{CEO}	20	30	40	50	Vdc
Collector to Base Voltage	BV_{CBO}	40	60	80	100	Vdc
Emitter to Base Voltage	BV_{EBO}	20	30	40	50	Vdc
Collector Current (Continuous)	I_C	15	15	15	15	amp
Collector Current (Peak)	I_C	20	20	20	20	amp
Collector Junction Temperature	T_j	100	100	100	100	°C
Collector Dissipation (25°C Mtg. Base Temp.)	P_C	90	90	90	90	watt

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typical	Maximum	Unit
Thermal Resistance	θ_{JC}	0.6	0.8	°C/W

ELECTRICAL CHARACTERISTICS, GENERAL (At 25°C Mounting Base Temperature)

Parameter		Symbol	Min	Typ	Max	Unit
Collector-Base Cutoff Current		I_{CBO}				
$V_{CB} = -25V$	2N1553, 2N1557		—	—	3.0	mA
$V_{CB} = -40V$	2N1554, 2N1558		—	—	3.0	mA
$V_{CB} = -55V$	2N1555, 2N1559		—	—	3.0	mA
$V_{CB} = -65V$	2N1556, 2N1560		—	—	3.0	mA
Collector-Base Cutoff Current $V_{CB} = -2V$ (all types)		I_{CBO}	—	—	200	μA

ELECTRICAL CHARACTERISTICS, GENERAL *(continued)*

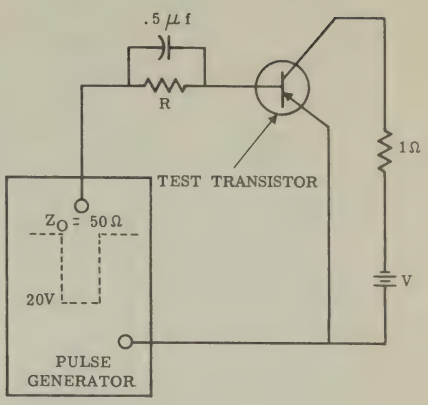
Parameter		Symbol	Min	Typ	Max	Unit
Collector-Base Cutoff Current		I_{CBO}				
at $T_B = +90°C$						
at $V_{CB} = ½ BV_{CES}$ rating			—	—	20	mA
Emitter-Base Cutoff Current		I_{EBO}				
$V_{EB} = 12V$ (all types)			—	—	0.5	mA
Collector-Emitter Breakdown Voltage		BV_{CES}				
$I_C = 300mA, V_{EB} = 0$						
	2N1553, 2N1557		30	—	—	volts
	2N1554, 2N1558		45	—	—	volts
	2N1555, 2N1559		60	—	—	volts
	2N1556, 2N1560		75	—	—	volts
Collector-Emitter Leakage Current		I_{CEX}				
$V_{BE} = 1.0V$						
$V_{CE} = 40$	2N1553, 2N1557		—	—	20	mA
$V_{CE} = 60$	2N1554, 2N1558		—	—	20	mA
$V_{CE} = 80$	2N1555, 2N1559		—	—	20	mA
$V_{CE} = 100$	2N1556, 2N1560		—	—	20	mA
Collector-Emitter Breakdown Voltage		BV_{CEO}				
$I_C = 300mA, I_B = 0$						
	2N1553, 2N1557		20	—	—	volts
	2N1554, 2N1558		30	—	—	volts
	2N1555, 2N1559		40	—	—	volts
	2N1556, 2N1560		50	—	—	volts
Collector-Base Breakdown Voltage		BV_{CBO}				
$I_C = 20mA$						
	2N1553, 2N1557		40	—	—	volts
	2N1554, 2N1558		60	—	—	volts
	2N1555, 2N1559		80	—	—	volts
	2N1556, 2N1560		100	—	—	volts

ELECTRICAL CHARACTERISTICS, COMMON EMITTER (At 25°C Mounting Base Temperature)

Characteristics	Symbol	Min	Typ	Max	Unit
Current Gain	h_{FE}				
$V_{CE} = -2V, I_C = 10A$					
2N1553, 2N1554, 2N1555, 2N1556		30	—	60	—
2N1557, 2N1558, 2N1559, 2N1560		50	—	100	—
Base-Emitter Drive Voltage	V_{BE}				
$I_C = 10A, I_B = 1.0A$					
2N1553, 2N1554, 2N1555, 2N1556		—	—	1.0	volts
2N1557, 2N1558, 2N1559, 2N1560		—	—	0.7	volts
Collector Saturation Voltage	$V_{CE(SAT)}$				
$I_C = 10A, I_B = 1.0A$					
2N1553, 2N1554, 2N1555, 2N1556		—	0.4	0.7	volts
2N1557, 2N1558, 2N1559, 2N1560		—	0.25	0.5	volts
Transconductance	g_{FE}				
$V_{CE} = -2V, I_C = 10A$					
2N1553, 2N1554, 2N1555, 2N1556		8	16	30	mhos
2N1557, 2N1558, 2N1559, 2N1560		12	20	40	mhos
Switching Characteristics					
$I_C = 10A$					
Delay + Rise Time (all types)	$t_d + t_r$	—	10	—	μsec
Storage Time (all types)	t_s	—	5	—	μsec
Fall Time (all types)	t_f	—	25	—	μsec
Frequency Cutoff	f_{ae}				
$V_{CE} = -2V, I_C = 5A$					
2N1553, 2N1554, 2N1555, 2N1556		—	6	—	kc
2N1557, 2N1558, 2N1559, 2N1560		—	5	—	kc

SWITCHING TIME MEASURING UNIT

	2N1553-56	2N1557-60
I_C (Amps)	10	10
V (Volts)	10	10
I_{ON} (ma)	666	400
R (ohms)	30	50
$t_d + t_r$ (μsec)	10	10
t_s (μsec)	5	5
t_f (μsec)	25	25



MILITARY TYPES

2N297A MIL-T-19500A/36 (Signal Corps) (See Case No. 1 – Derating Curve No. 2)

The Motorola type 2N297A is a germanium PNP alloy-junction power transistor designed for general purpose industrial and military applications where extremely high reliability is mandatory. They are specified in such a manner as to assure control of the most important characteristics for both linear and switching applications.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Min	Unit
Collector to Base Voltage	BV_{CBO}	80	Vdc
Emitter to Base Voltage	BV_{EBO}	40	Vdc
Operating Temperature Range*	—	−65° to +95°	°C
Collector Dissipation for Mounting Base Temperature of 75°C*	P_C	30	watt

*Motorola Transistor Ratings — $T_J = 100°C$, $P_C = 90$ watts with case at 25°C.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
DC Current Gain $V_{CE} = 2V, I_C = .5$ A	h_{FE}	40	100	—
DC Current Gain $V_{CE} = 2V, I_C = 2.0$ A	h_{FE}	20	—	—
Current Gain Frequency Cutoff Small Signal $V_{CE} = 14Vdc, I_C = .5$ amp	f_{ae}	5	—	kc

GROUP A INSPECTION — TABLE I

(at 25°C ±3°C mounting base temperature unless otherwise specified)

Examination or Test	Conditions	AQL % Defective	Inspection Level	Symbol	Limits Max	Limits Min	Unit
Subgroup 1							
Visual and Mechanical Examination	—	1.0	II	—	—	—	—
Subgroup 2							
Emitter Cutoff Current	V_{EB} = 40 Vdc, I_C = 0			I_{EBO}	—	3.0	mAdc
Collector Cutoff Current	V_{CB} = 2 Vdc, I_E = 0			I_{CBO}	—	200	μAdc
Collector Cutoff Current	V_{CB} = 60 Vdc, I_E = 0			I_{CBO}	—	3.0	mAdc
Base Current	V_{CE} = 2 Vdc, I_C = 0.5 Adc			I_B	5.0	12.5	mAdc
Base Current	V_{CE} = 2 Vdc, I_C = 2 Adc			I_B	—	100	mAdc
Base Voltage	V_{CE} = 2 Vdc, I_C = 2 Adc	1.0	II	V_{EB}	—	1.5	Vdc
Floating Potential	V_{CB} = 60 Vdc, Voltmeter Input R = 10 meg. min.			V_{f1}	0.0	180	mVdc
Collector Voltage (Saturation)	I_C = 2 Adc, I_B = 200 mAdc			$V_{CE(SAT)}$	0.0	1.0	Vdc
Collector Voltage	I_C = 300 mAdc, I_B = 0			BV_{CEO}	40.0	—	Vdc
Collector Voltage	I_C = 300 mAdc, V_{EB} = 0			BV_{CES}	50.0	—	Vdc
Subgroup 3							
Small-Signal Short-Circuit Forward-Transfer Current-Ratio Cutoff Frequency	V_{CE} = 14.0 Vdc, I_C = 0.5 Adc	4.0	II	$f_{\alpha e}$	5	—	kc
High-Temperature Operation	TB = +71°C (min)			—	—		—
Collector Cutoff Current	V_{CB} = 30 Vdc, I_E = 0			I_{CBO}	—	6.0	mAdc

2N1011 MIL-T-19500A/67 (Signal Corps)

(See Case No. 1 ~ Derating Curve No. 2)

The Motorola type 2N1011 is a germanium PNP alloy-junction power transistor designed for general purpose industrial and military applications where extremely high reliability is mandatory. They are specified in such a manner as to assure control of the most important characteristics for both linear and switching applications.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Min	Unit
Collector to Base Voltage	BV_{CBO}	80	Vdc
Emitter to Base Voltage	BV_{EBO}	40	Vdc
Emitter Current	I_E	5.0	amp

ABSOLUTE MAXIMUM RATINGS *(continued)*

Characteristic	Symbol	Min	Unit
Operating Temperature Range*	—	−65° to +95°	°C
Collector Dissipation for Mounting Base Temperature of 75°C*	P_C	30	watt

*Motorola Transistor Ratings — $T_J = 100°C$, $P_C = 90$ watts with case at 25°C.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
DC Current Gain $V_{CE} = 2V, I_C = 1.0$ A	h_{FE}	—	150	—
DC Current Gain $V_{CE} = 2V, I_C = 3.0$ A	h_{FE}	30	75	—
Current Gain Frequency Cutoff Small Signal $V_{CE} = 2$Vdc, $I_C = 3$ amp	f_{ae}	5	—	kc

GROUP A INSPECTION — TABLE I

Examination or Test	Conditions	AQL % Defective	Inspection Level	Symbol	Limits Min	Limits Max	Unit
Subgroup 1							
Visual and Mechanical Examination	—	1.0	II	—	—	—	—
Subgroup 2							
Emitter Cutoff Current	$V_{EB} = 40$ Vdc, $I_C = 0$			I_{EBO}	—	3.0	mAdc
Collector Cutoff Current	$V_{CB} = 2$ Vdc, $I_E = 0$			I_{CBO}	—	200	μAdc
Collector Cutoff Current	$V_{CB} = 80$ Vdc, $I_E = 0$			I_{CBO}	—	15.0	mAdc
Base Current	$V_{CE} = 2$ Vdc, $I_C = 1$ Adc			I_B	6.7	—	mAdc
Base Current	$V_{CE} = 2$ Vdc, $I_C = 3$ Adc			I_B	40	100	mAdc
Base Voltage	$V_{CE} = 2$ Adc, $I_C = 3$ Adc	1.0	II	V_{EB}	—	2.0	Vdc
Floating Potential	$V_{CB} = 80$ Vdc, Voltmeter Input Resistance = 10 meg. min.			V_{f1}	—	1.0	Vdc
Collector Voltage (Saturation)	$I_C = 3$ Adc, $I_B = 200$ mAdc			$V_{CE(SAT)}$	0.0	1.5	Vdc
Collector Voltage	$I_C = 300$ mAdc, $I_B = 0$			BV_{CEO}	40	—	Vdc
Collector Voltage	$I_C = 300$ mAdc, $V_{EB} = 0$			BV_{CES}	80	—	Vdc
Subgroup 3							
Small-Signal Short-Circuit Forward-Transfer Current-Ratio Cutoff Frequency	$V_{CE} = 2$ Vdc, $I_C = 3$ Adc			F_{ae}	5	—	kc
High-Temperature Operation	TB = +90°C (min)	4.0	II				
Collector Cutoff Current	$V_{CB} = 30$ Vdc, $I_E = 0$			I_{CBO}	—	20	mAdc

2N1120 MIL-T-19500A/68 (Signal Corps)

(See Case No. 2 — Derating Curve No. 2)

The Motorola type 2N1120 is a germanium PNP, alloy-junction power transistor designed for general purpose industrial and military applications where extremely high reliability is mandatory. They are specified in such a manner as to assure control of the most important characteristics for both linear and switching applications.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Min	Unit
Collector to Base Voltage	BV_{CBO}	80	Vdc
Emitter to Base Voltage	BV_{EBO}	40	Vdc
Emitter Current	I_E	15	amp
Operating Temperature Range*	—	—65° to +95°	°C
Collector Dissipation for Mounting Base Temperature of 25°C*	P_C	45	watt

*Motorola Transistor Ratings — $T_J = 100°C$, $P_C = 90$ watts with case at 25°C.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
DC Current Gain $V_{CE} = 2V, I_C = 5.0Adc$	h_{FE}	—	100	—
DC Current Gain $V_{CE} = 2V, I_C = 10.0Adc$	h_{FE}	10	50	—
Current Gain Frequency Cutoff Small Signal $V_{CE} = 2Vdc, I_C = 5$ amps	f_{ae}	5	—	kc

GROUP A INSPECTION — TABLE I

(at 25°C ±3°C mounting base temperature unless otherwise specified)

Examination or Test	Conditions	AQL % Defective	Inspection Level	Symbol	Limits Min	Limits Max	Unit
Subgroup 1 Visual and Mechanical Examination	—	1.0	II	—	—	—	—
Subgroup 2							
Emitter Cutoff Current	$V_{EB} =$ 40 Vdc, $I_C =$ 0			I_{EBO}	—	5.0	mAdc
Collector Cutoff Current	$V_{CB} =$ 2 Vdc, $I_E =$ 0			I_{CBO}	—	300	μAdc
Collector Cutoff Current	$V_{CB} =$ 80 Vdc, $I_E =$ 0			I_{CBO}	—	15.0	mAdc
Base Current	$V_{CE} =$ 2 Vdc, $I_C =$ 5 Adc			I_B	50	—	mAdc
Base Current	$V_{CE} =$ 2 Vdc, $I_C =$ 10 Adc			I_B	200	1,000	mAdc
Base Voltage	$V_{CE} =$ 2 Vdc, $I_C =$ 10 Adc	1.0	II	V_{EB}	—	2.0	Vdc

GROUP A INSPECTION — TABLE I *(continued)*

Examination or Test	Conditions	AQL % Defective	Inspection Level	Symbol	Limits Min	Limits Max	Unit
Floating Potential	V_{CB} = 80 Vdc Voltmeter Input R = 10 meg. min.			V_{f1}	—	1.0	Vdc
Collector Voltage (Saturation)	I_C = 10 Adc I_B = 1 Adc			$V_{CE(SAT)}$	—	1.0	Vdc
Base Voltage (saturation)	I_B = 1 Adc I_C = 10 Adc			V_{BE}	—	1.5	Vdc
Collector Voltage	I_C = 300 mAdc I_B = 0			BV_{CEO}	40	—	Vdc
Collector Voltage	I_C = 300 mAdc V_{EB} = 0			BV_{CES}	70	—	Vdc
Subgroup 3							
Small-Signal Short-Circuit Forward-Transfer Current-Ratio Cutoff Frequency	V_{CE} = 2 Vdc I_C = 5 Adc	4.0	II	F_{ae}	3	—	kc
High-Temperature Operation	TB = +90°C (min)						
Collector Cutoff Current	V_{CB} = 30 Vdc I_E = 0			I_{CBO}	—	20	mAdc

AUTOMOTIVE POWER TRANSISTORS

2N176, 2N669 (See Case No. 4 – Derating Curve No. 3)

Motorola types 2N176 and 2N669 are germanium PNP, alloy-junction transistors designed for high power gain and low distortion in audio-frequency applications and graded for closely controlled power gain ranges.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Collector to Base Voltage	BV_{CBO}	40	volts
Collector Current (based on maximum at which characteristics are specified. Permanent damage will not result if this rating and no other is exceeded)	I_C	3	amps
*Collector Dissipation At 80° Mounting Base Temperature Derate 1.0 watt/°C rise	P_C	10	watts
Collector Junction Temperature	T_J	90	°C

*See power-temperature derating curve

ELECTRICAL CHARACTERISTICS — GENERAL

at mounting base temperature 25°C ± 3°C except where noted

Characteristic	Symbol	Min	Typ	Max	Unit
Collector Cutoff Current	I_{CBO}				
$V_{CB} = 30V$		—	—	3.0	ma
$V_{CB} = 2V$		—	50	—	μa
$V_{CB} = 30V$, T = 90°C		—	—	20.0	ma
Emitter Cutoff Current	I_{EBO}				
$V_{EB} = 10V$		—	—	2.0	ma
Collector Breakdown Voltage	BV_{CES}				
$I_C = 330ma$		30	—	—	volts

THERMAL CHARACTERISTICS — TYPICAL

Characteristic	Symbol	Typ	Unit
Thermal Resistance Junction to Case	θ_{JC}	0.7	°C/W

ELECTRICAL CHARACTERISTICS — COMMON EMITTER

at mounting base temperature 25°C ± 3°C except where noted

		2N176			2N669			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Power Gain, (± 0.5db) $P_O = 2$ watts, $V_{CE} = 12V$, $I_C = 0.5A$, f = 1 kc, $R_S = 10$ ohms, $R_L = 26.6$ ohms	G_e	34	35	37	38	40	—	db
Total Harmonic Distortion under same conditions as power gain	—	—	—	5	—	—	5	%
DC Forward Current Gain $V_{CE} = 2V$, $I_C = 0.5A$	h_{FE}	25	—	90	—	100	250	—
Current Gain Frequency Cutoff $V_{CE} = 12V$, $I_C = 0.5A$, f = 1 kc (ref)	f_{ae}	4	7	—	3	5	—	kc
Small Signal Forward Current Gain f = 1 kc, $V_{CE} = 2V$, $I_C = 0.5A$	h_{fe}	—	45	—	—	90	—	—
Small Signal Input Impedance f = 1 kc, $V_{CE} = 2V$, $I_C = 0.5A$	h_{ie}	8	16	25	—	20	50	ohms
Collector Saturation Voltage $I_C = 3A$, $I_B = 300$ ma	$V_{CE(SAT)}$	—	0.4	—	—	0.4	—	volts

2N350A, 2N351A, 2N376A (See Case No. 4– Derating Curve No. 3)

Motorola types 2N350A, 2N351A and 2N376A are germanium PNP, alloy-junction transistors designed and specified for general purpose industrial applications. Units are controlled for high power gain and low distortion at output levels up to 4 watts Class A and 15 watts Class B. Power switching characteristics are controlled up to 3, 4 and 5 amps respectively. Packaged in Motorola's industry standard power transistor case, these units are easy to mount and capable of withstanding very high shock and vibration levels.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Collector to Base Voltage	BV_{CBO}	50	volts
Collector to Emitter Voltage	BV_{CES}	40	volts
Collector Dissipation at 70° Mounting Base Temperature Derate 1.2°C/W	P_C	25	watts
Collector Junction Temperature	T_J	100	°C

ELECTRICAL CHARACTERISTICS at mounting base temperature 25°C ± 3°C except where noted

Characteristic	Symbol	Min	Typ	Max	Unit
Collector Cutoff Current	I_{CBO}				
$V_{CB} = 30V$		—	—	3.0	ma
$V_{CB} = 2V$		—	50	—	μa
$V_{CB} = 30V, T = 100°C$		—	—	30	ma
Emitter Cutoff Current	I_{EBO}				
$V_{EB} = 10V$		—	—	2.0	ma
Collector Breakdown Voltage	BV_{CES}				
$I_C = 1A$ (This test should be made under dynamic conditions only)		40	—	—	volts

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Thermal Resistance Junction to Case	θ_{JC}	—	.7	1.2	°C/W

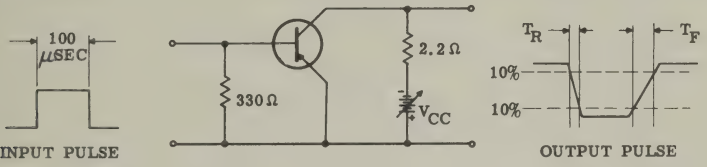
ELECTRICAL CHARACTERISTICS — COMMON EMITTER at mounting base temperature 25°C ± 3°C

Characteristic	Symbol	2N350A			2N351A			2N376A			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Gain, (± 0.5db) $P_o = 4$ watts $V_{CE} = 12V$, $I_C = 0.7A$, $f = 1kc$ $R_S = 10$ ohms, $R_L = 15$ ohms	G_e	30	—	33	32	—	35	34	—	37	db
Total Harmonic Distortion under same conditions as power gain		—	—	7%	—	—	7%	—	—	7%	—
DC Forward Current Gain $V_{CE} = 2V$, $I_C = 0.7A$	h_{FE}	20	—	60	25	—	90	35	—	120	—
Current Gain Frequency Cutoff $V_{CE} = 12V$, $I_C = 0.7A$, $f = 1kc$ (REF)	$f_{\alpha e}$	5	—	—	5	—	—	5	—	—	kc
Small Signal Forward Current Gain $f = 1kc$, $V_{CE} = 2V$, $I_C = 0.7A$	h_{fe}	—	30	—	—	45	—	—	60	—	—
Small Signal Input Impedance $f = 1kc$, $V_{CE} = 2V$, $I_C = 0.7A$	h_{ie}	5	—	17	6	—	20	7	—	25	ohms
Collector Saturation Voltage $I_C = 3A$, $I_B = 300$ ma	$V_{CE(SAT)}$	—	.8	1.75	—	—	—	—	—	—	volts
Base to Emitter Voltage $I_C = 3A$, $I_B = 300$ ma	V_{EB}	—	1.0	2.00	—	—	—	—	—	—	volts
Collector Saturation Voltage $I_C = 4A$, $I_B = 400$ ma	$V_{CE(SAT)}$	—	—	—	—	.8	1.75	—	—	—	volts
Base to Emitter Voltage $I_C = 4A$, $I_B = 400$ ma	V_{EB}	—	—	—	—	1.0	2.00	—	—	—	volts
Collector Saturation Voltage $I_C = 5A$, $I_B = 500$ ma	$V_{CE(SAT)}$	—	—	—	—	—	—	—	.8	1.75	volts
Base to Emitter Voltage $I_C = 5A$, $I_B = 500$ ma	V_{EB}	—	—	—	—	—	—	—	1.0	2.00	volts

TYPICAL SWITCHING CHARACTERISTICS

at 25°C mounting base temperature in circuit illustrated below

Characteristic	Symbol	2N350A	2N351A	2N376A	Unit
Load Resistance	R_L	2.2	2.2	2.2	ohms
"On" Collector Current (V_{CC} supply adjusted to give desired current)	I_C	3	4	5	amp
"On" Base Current	I_B	0.3	0.4	0.5	amp
Rise Time	T_R	5.0	4.5	4.0	μsec
Fall Time	T_F	37	40	42	μsec



Motorola Industrial Low-Silhouette TO-36 Power Transistor

2N174, 2N1100, 2N1358 (Case TO-36, Derating Curve 4)

Motorola types 2N174, 2N1100, and 2N1358 are germanium PNP power transistors designed for applications requiring high power dissipation up to 150 watts. They are furnished in the new "low-silhouette" TO-36 package.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	2N174	2N1100	2N1358	Unit
Collector Diode Voltage	BV_{CB}	80	100	80	Vdc
Emitter-to-Base Voltage	BV_{EBO}	60	80	60	Vdc
Emitter Current (Continuous)	I_E	15	15	15	amp
Base Current (Continuous)	I_B	4	4	4	amp
Maximum Junction Temperature	$T_{j\,max}$	+100	+100	+100	°C
Minimum Junction Temperature	$T_{j\,min}$	−65	−65	−65	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typical	Maximum	Units
Thermal Resistance (Junction to case)	θ_{JC}	0.4	0.5	°C/W

ELECTRICAL CHARACTERISTICS, GENERAL

Characteristic		Symbol	Min	Typical	Max	Unit
Collector-to-Base Cutoff Current		I_{CBO}				
	2N174		—	100	—	μA
($V_{CBO} = -2$ volts)	2N1100		—	100	—	μA
	2N1358		—	100	200	μA
Collector-to-Base Cutoff Current		I_{CB}				
($V_{EB} = -1.5$ volts, $V_{CB} = -80$ volts)	2N174		—	2	8	mA
-100	2N1100		—	2	8	mA
-80	2N1358		—	2	8	mA
Emitter-to-Base Cutoff Current		I_{EBO}				
($V_{EBO} = -60$ volts)	2N174		—	1	8	mA
-80	2N1100		—	1	8	mA
-60	2N1358		—	1	8	mA
Collector-to-Base Cutoff Current		I_{CBO}				
($V_{CBO} = -80$ volts, 71°C)	2N174		—	—	15	mA
-100	2N1100		—	—	15	mA
-60	2N1358		—	4	6	mA
Emitter-to-Base Cutoff Current		I_{EBO}				
($V_{EBO} = -30$ volts, 71°C)	2N1358		—	4	6	mA
Floating Potential		V_{BE}				
($I_E = 0$, $V_{CBO} = -80$ volts)	2N174		—	—	1.0	volt
-100	2N1100		—	—	1.0	volt
-80	2N1358		—	0.15	1.0	volt
Current Gain		h_{FE}				
($V_{CE} = -2$ volts, $I_C = 1.2$ amp)	2N1358		40	55	80	—
($V_{CE} = -2$ volts, $I_C = 5$ amp)	2N174		25	—	50	—
	2N1100		25	—	50	—
	2N1358		25	35	—	—
-2 volts, ($I_C = 12$ amp)	2N174		—	20	—	—
	2N1100		—	20	—	—
Emitter-to-Base Voltage		V_{EB}				
($V_{CB} = -2$ volts, $I_C = 1.2$ amp)	2N1358		—	0.35	0.5	Vdc
-2 volts, ($I_C = 5$ amp)	2N174		—	0.65	0.9	Vdc
	2N1100		—	0.65	0.9	Vdc
	2N1358		—	0.65	0.9	Vdc
Saturation Voltage		$V_{CE(sat)}$				
($I_B = 2$ amp, $I_C = 12$ amp)	2N174		—	0.3	0.9	Vdc
	2N1100		—	0.3	0.7	Vdc
	2N1358		—	0.3	0.7	Vdc
Collector-to-Emitter Voltage *		BV_{CES}				
($I_C = 300$ mA, $V_{EB} = 0$)*	2N174		—70	—	—	Vdc
	2N1100		—80	—	—	Vdc
	2N1358		—70	—	—	Vdc
Collector-to-Emitter Voltage *		BV_{CEO}				
($I_C = 1.0$ amp, $I_B = 0$	2N174		—55	—	—	Vdc
1.0 amp, $I_B = 0$	2N1100		—65	—	—	Vdc
300 mA, $I_B = 0$	2N1358		—40	—	—	Vdc
Common-Emitter Current Amplification Cutoff Frequency		f_{α_e}				
($I_C = 5$ amp, $V_{CB} = 6$ volts)	2N174 2N1100		—	10	—	kc
Common-Base Current Amplification Cutoff Frequency		f_{α_b}				
($I_C = 1$ amp, $V_{CB} = -12$ volts)	2N1358		100	—	—	kc

ELECTRICAL CHARACTERISTICS, GENERAL *(continued)*

Characteristic		Symbol	Min	Typ	Max	Unit
Rise Time ("on" $I_C = 12$ Adc, $I_B = 2$ Adc, $V_{CE} = -12$ volts)	All Types	t_r	—	15	—	μsec
Fall Time ("off" $I_C = 0$, $V_{EB} = -6$ volts, $R_{EB} = 10$ ohms)	All Types	t_f	—	15	—	μsec

* In order to avoid excessive heating of the collector junction, perform test by the sweep method. (not BV_{CEO} on 2N1358)

2N277, 2N278, 2N173, 2N1099 (Case 5, Derating Curve 4)

Motorola types 2N277, 2N278, 2N173, and 2N1099 are germanium PNP power transistors designed for applications requiring high power dissipation up to 150 watts. They are furnished in the new "low-silhouette" TO-36 package.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	2N277	2N278	2N173	2N1099	Unit
Collector-to-Base Voltage	BV_{CB}	40	50	60	80	Vdc
Emitter-to-Base Voltage	BV_{EBO}	20	30	40	40	Vdc
Emitter Current (Continuous)	I_E	15	15	15	15	amp
Base Current (Continuous)	I_B	4	4	4	4	amp
Maximum Junction Temperature	$T_{j\,max}$	+100	+100	+100	+100	°C
Minimum Junction Temperature	$T_{j\,min}$	−65	−65	−65	−65	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typical	Maximum	Units
Thermal Resistance (Junction to case)	θ_{JC}	0.4	0.5	°C/W

ELECTRICAL CHARACTERISTICS, GENERAL (at 25°C Mounting Base Temperature)

Characteristic		Symbol	Min	Typical	Max	Unit
Collector-to-Base Cutoff Current		I_{CBO}				
($V_{CBO} = -2$ volts)	All Types		—	100	—	μA
Collector-to-Base Cutoff Current		I_{CB}				
($V_{EB} = -1.5$ volts, $V_{CB} = -40$ volts)	2N277		—	2	8	mA
−50	2N278		—	—	—	mA
−60	2N173		—	—	—	mA
−80	2N1099		—	—	—	mA
Emitter-to-Base Cutoff Current		I_{EBO}				
($V_{EBO} = -20$ volts)	2N277		—	1	8	mA
−30	2N278		—	—	—	mA
−40	2N173		—	—	—	mA
−40	2N1099		—	—	—	mA
Collector-to-Base Cutoff Current		I_{CBO}				
($V_{CBO} = -40$ volts, 71°C)	2N277		—	—	15	mA
−50	2N278		—	—	—	mA
−60	2N173		—	—	—	mA
−80	2N1099		—	—	—	mA
Floating Potential		V_{BE}				
($I_E = 0$, $V_{CBO} = -40$ volts)	2N277		—	0.15	1.0	volt
−50	2N278		—	—	—	volt
−60	2N173		—	—	—	volt
−80	2N1099		—	—	—	volt
Current Gain		h_{FE}				
($V_{CE} = -2$ volts, $I_C = 5$ amp)	All Types		35	—	70	—
($V_{CE} = -2$ volts, $I_C = 12$ amp)			—	25	—	—
Emitter-to-Base Voltage		V_{EB}				
($V_{CB} = -2$ volts, $I_C = 5$ amp)	2N277		—	0.65	—	Vdc
	2N278		—	0.65	—	Vdc
	2N173		—	0.65	—	Vdc
	2N1099		—	0.65	0.9	Vdc
Saturation Voltage		$V_{CE(SAT)}$				
($I_B = 2$ amp, $I_C = 12$ amp)	2N277		—	0.3	—	Vdc
	2N278		—	0.3	1.0	Vdc
	2N173		—	0.3	1.0	Vdc
	2N1099		—	0.3	0.7	Vdc
Collector-to-Emitter Voltage *		BV_{CES}				
($I_C = 300$ mA, $V_{EB} = 0$)	2N277		−40	—	—	Vdc
	2N278		−45	—	—	Vdc
	2N173		−50	—	—	Vdc
	2N1099		−70	—	—	Vdc
Collector-to-Emitter Voltage *		BV_{CEO}				
($I_C = 1$ amp, $I_B = 0$)	2N277		−25	—	—	Vdc
	2N278		−30	—	—	Vdc
	2N173		−45	—	—	Vdc
	2N1099		−55	—	—	Vdc
Common-Emitter Current Amplification Cutoff Frequency		f_{α_b}				
($I_C = 5$ amp, $V_{CB} = -6$ volts)	All Types		—	10	—	kc
Rise Time ("on" $I_C = 12$ Adc,		t_r				
$I_B = 2$ Adc, $V_{CE} = -12$ volts)	All Types		—	15	—	μsec
Fall Time ("off" $I_C = 0$,		t_f				
$V_{EB} = -6$ volts, $R_{EB} = 10$ ohms)	All Types		—	15	—	μsec

* To avoid excessive heating of the collector junction, perform these tests with the sweep method.

2N441 THRU 2N443 (Case TO-36, Derating Curve 4)

Motorola types 2N441 thru 2N443 are germanium PNP power transistors designed for applications requiring high power dissipation up to 150 watts. They are furnished in the new "low-silhouette" TO-36 package.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	2N441	2N442	2N443	Unit
Collector-to-Base Voltage	BV_{CB}	40	50	60	Vdc
Emitter-to-Base Voltage	BV_{EBO}	20	30	40	Vdc
Emitter Current (Continuous)	I_E	15	15	15	amp
Base Current (Continuous)	I_B	4	4	4	amp
Maximum Junction Temperature	$T_{j\,max}$	+100	+100	+100	°C
Minimum Junction Temperature	$T_{j\,min}$	−65	−65	−65	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typical	Maximum	Units
Thermal Resistance (Junction to case)	θ_{JC}	0.4	0.5	°C/W

ELECTRICAL CHARACTERISTICS, GENERAL

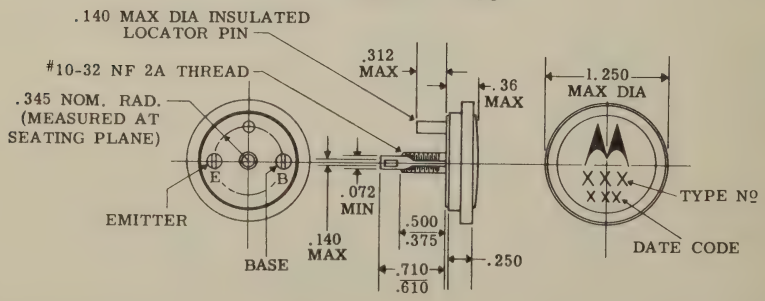
Characteristic		Symbol	Min	Typical	Max	Unit
Collector-to-Base Cutoff Current ($V_{CBO} = -2$ volts)	All Types	I_{CBO}	—	100	—	μA
Collector-to-Base Cutoff Current ($V_{EB} = -1.5$ volts, $V_{CB} = -40$ volts)	2N441	I_{CB}	—	2	8	mA
−50	2N442		—	2	8	mA
−60	2N443		—	2	8	mA
Collector-to-Base Cutoff Current (71°C, $V_{CBO} = -40$ volts)	2N441	I_{CBO}	—	—	15	mA
−50	2N442		—	—	15	mA
−60	2N443		—	—	15	mA

ELECTRICAL CHARACTERISTICS, GENERAL *(continued)*

Characteristic		Symbol	Min	Typical	Max	Unit
Emitter-to-Base Cutoff Current		I_{EBO}				
($V_{EBO} = -20$ volts)	2N441		—	1	8	mA
-30	2N442		—	1	8	mA
-40	2N443		—	1	8	mA
Collector-to-Emitter Voltage *		BV_{CES}				
($V_{EB} = 0$, $I_C = 300$ mA)	2N441		—40	—	—	Vdc
	2N442		—45	—	—	Vdc
	2N443		—50	—	—	Vdc
Collector-to-Emitter Voltage *		BV_{CEO}				
($I_C = 1$ amp, $I_B = 0$)	2N441		—25	—	—	Vdc
	2N442		—30	—	—	Vdc
	2N443		—45	—	—	Vdc
Floating Potential		V_{BE}				
($I_E = 0$, $V_{CB} = -40$ volts)	2N441		—	—	1.0	volt
-50	2N442		—	—	1.0	volt
-60	2N443		—	—	1.0	volt
Current Gain		h_{FE}				
($I_C = 5$ amp, $V_{CE} = -2$ volts)	All Types		20	—	40	—
$I_C = 12$ amp, $V_{CE} = -2$	All Types		—	20	—	—
Emitter-to-Base Voltage		V_{EB}				
($I_C = 5$ amp, $V_{CB} = -2$ volts)	2N441		—	0.65	—	Vdc
	2N442		—	0.65	—	Vdc
	2N443		—	0.65	0.9	Vdc
Saturation Voltage		$V_{CE(sat)}$				
($I_C = 12$ amp, $I_B = 2$ amp)	2N441		—	0.3	—	Vdc
	2N442		—	0.3	—	Vdc
	2N443		—	0.3	1.0	Vdc
Common-Emitter Current Amplification Cutoff Frequency		f_{α_e}				
($I_C = 5$ amp, $V_{CE} = -6$ volts)	All Types		—	10	—	kc
Rise Time (on $I_C = 12$ Adc,		t_r				
$I_B = 2$ Adc, $V_{CE} = -12$ volts)	All Types		—	15	—	μsec
Fall Time (off $I_C = 0$,		t_f				
$V_{EB} = -6$ volts, $R_{EB} = 10$ ohms)	All Types		—	15	—	μsec

*To avoid excessive heating of the collector junction, perform test with the sweep method.

Case No. TO-36



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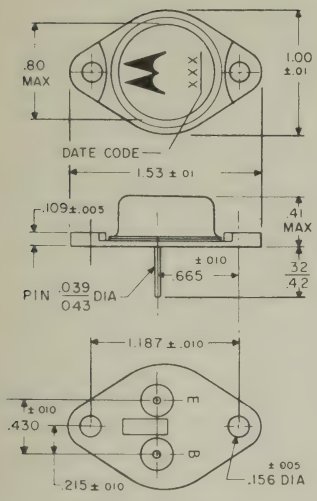

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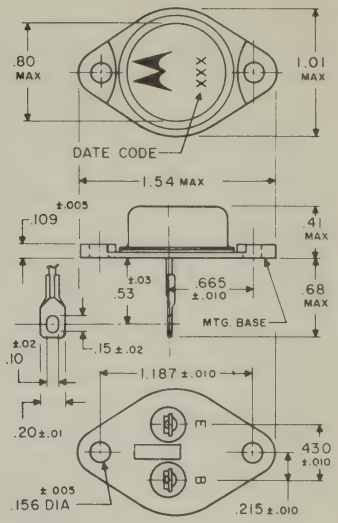

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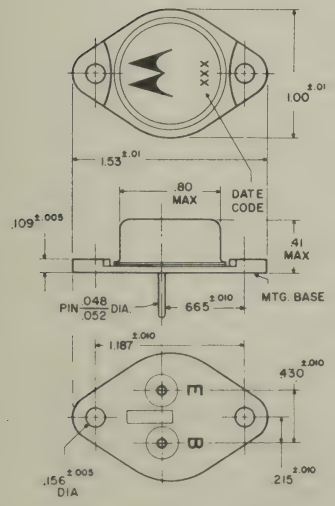

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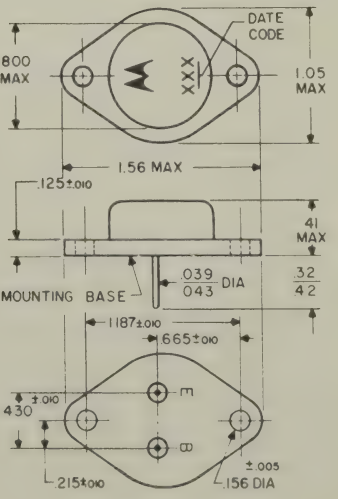
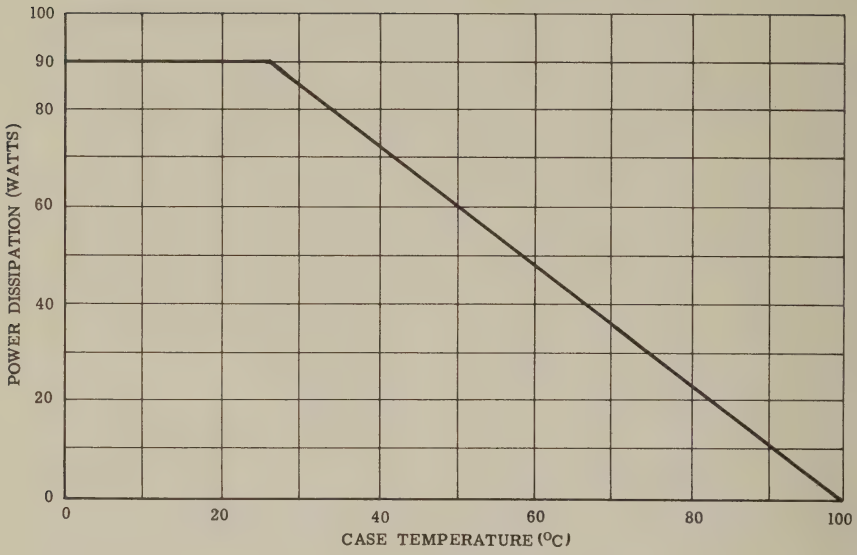


Derating Curve No. 1



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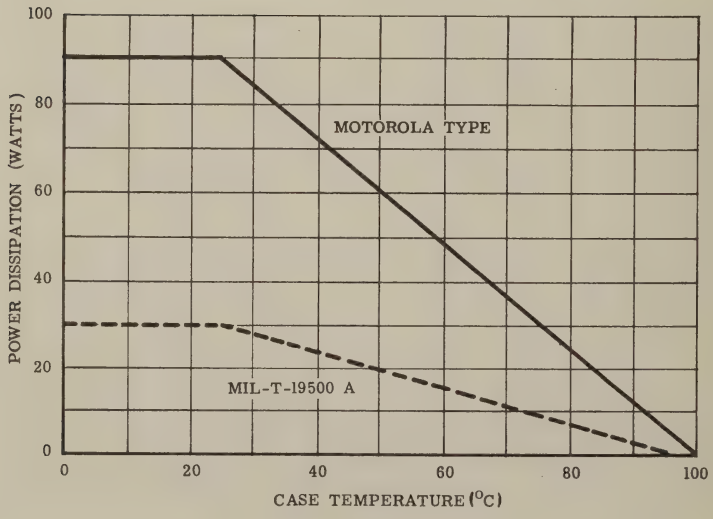
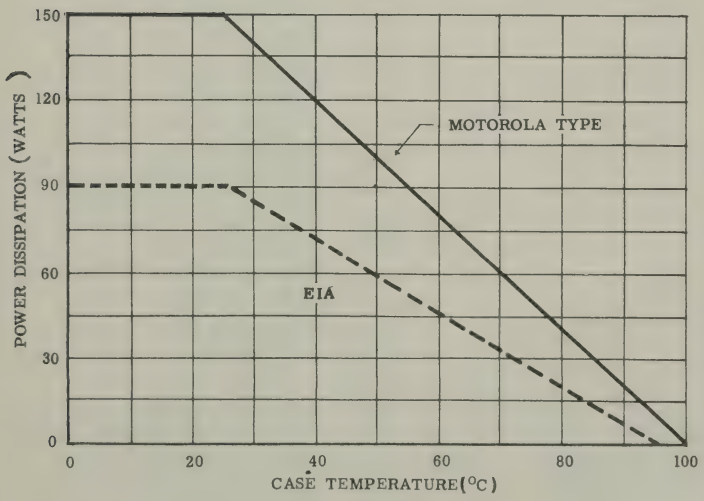


Derating Curve No. 3

Derating Curve No. 4



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INDEX

NOTES

ERRATA

Page 12 — In Section 2-5 common base frequency cutoff symbol should be $f_{\alpha b}$ instead of $f_{\alpha e}$.

Page 51 — Last line should also include I_E min.

Page 53 — In top line R_3 should read R_B.

Page 56 — Delete note following Equation 3-21.

Page 66 — Delete prime over R in Equation 3-43.

Page 67 — Figure reference following Equation 3-51 should be Figure 3-22.

Page 75 — Equation on Figure 3-35 should read:

$$P_{oPP} = \frac{2(V_{CE})^2}{R_{cc}}$$

Class A and B.

Page 93 — Figure 3-64 should read: Figure 3-65 — Power Response at 1% Total Harmonic Distortion (0 db = 2.0 Watts). Ordinate should read: Power Response (db).

Page 94 — Figure 3-65 should read: Figure 3-64 — Effect of Bypass Capacitor on Frequency Response at 0.5-Watt Level. Ordinate should read: Voltage Gain (db).

Page 143 — I_{BB} should read I_{B3}.

Page 144 — 2N1166 in last paragraph should read 2N1164.

Page 145 — 2N1166 in Figures 6-7 and 6-8 should read 2N1164.

Page 167 — In Temperature Derating Curve at bottom of page dashed line should taper down from 3 watts at 25°C to zero at 100°C.

Page 178 — In Electrical Characteristics values are given for I_{CBO}, BV_{CES}, I_{CEX}, BV_{CEO}, and BV_{CBO} for

2N1529, 2N1534
2N1530, 2N1535
2N1531, 2N1536
2N1532, 2N1537
2N1533, 2N1538

respectively, instead of 2N1529—2N1538.

Page 179 — In Electrical Characteristics values are given for

2N1529 thru 2N1533
2N1534 thru 2N1538

respectively, instead of 2N1529—2N1538.

Pages 180-181 — In Electrical Characteristics values are given for I_{CBO}, BV_{CES}, I_{CEX}, BV_{CEO}, and BV_{CBO} for

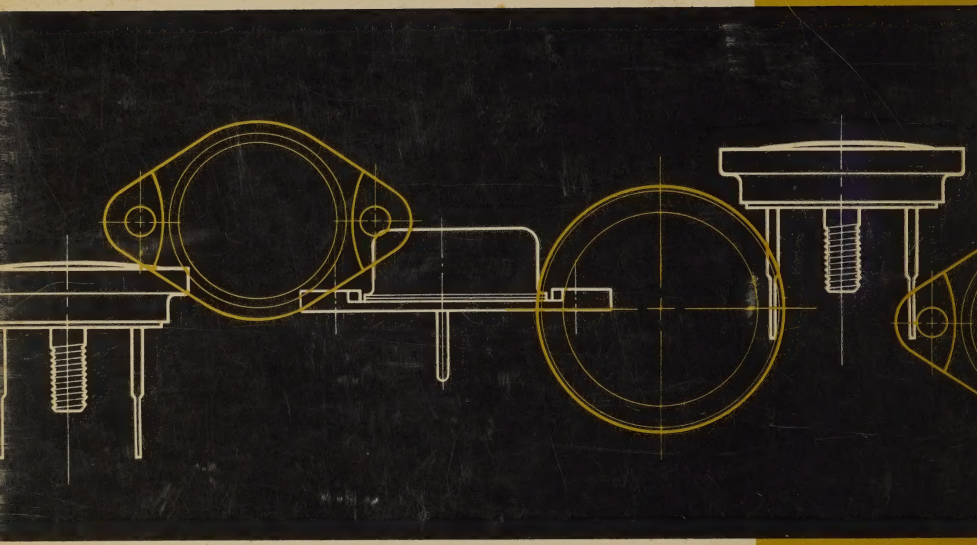
2N1539, 2N1544
2N1540, 2N1545
2N1541, 2N1546
2N1542, 2N1547
2N1543, 2N1548

respectively, instead of 2N1539—2N1548.

Page 182 — In Electrical Characteristics values are given for

2N1539 thru 2N1543
2N1544 thru 2N1548

respectively, instead of 2N1539—2N1548.



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